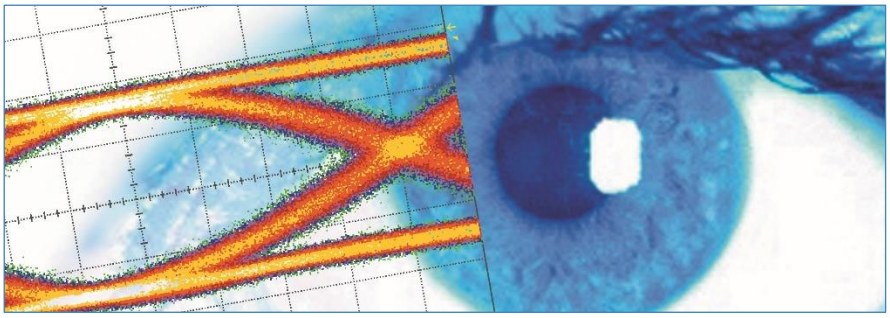


Data Sheet

SHF 12106 A

Bit Pattern Generator

Description

The SHF 12106 A is a synchronized multi-channel 64 Gbps bit pattern generator (BPG). It generates binary digital bit sequences such as pseudo-random bit sequences (PRBS) or user defined bit patterns.

The generated data patterns cover operating bit rates from 6 to 64 Gbps, continuously without gaps. Depending on the configuration, the instrument features up to four independent 64 Gbps differential channels (8 outputs).

The operating bit rate is set by the clock signal from an external clock source. The outputs can operate at either full clock or half clock, e.g., either a 64 GHz or a 32 GHz clock signal can be used for 64 Gbps operation.

The SHF 12106 A can be remote controlled via an Ethernet interface either by use of the SHF Control Center software provided by SHF or by custom software.

Further to the mode of operation as a multi-channel binary BPG, the functionality can be easily extended by attaching one of SHF's extender heads:

- By using a DAC such as the SHF 4-Bit DAC the easy-to-use graphical user interface enables the generation of arbitrary signals and the system becomes a fully functional AWG.
- In case a multiplexer (MUX) extender head is attached, 120 Gbps NRZ signals can be brought as close as possible to the DUT.
- PAM4 signals up to 128 GBaud (256 Gbps) can be generated by attaching the PAM4 multiplexer (PAM-MUX).

Features

- One to four 64 Gbps high quality differential data output channels
- Broadband operation up to an aggregated bit rate of 256 Gbps
- Built-in PRBS patterns and 16 Gbit user pattern per channel to support user defined patterns
- Standard Patterns such as JP03A, JP03B, QPRBS13, PRBS13Q, PRBS31Q, SSPRQ, Transmitter Linearity, SSPR, etc. are included and can be generated with combined signals
- All channels synchronized and independent
- Outputs adjustable up to -6 dB
- All outputs can be used single ended or differential
- Skew adjustment for each differential output
- Bit shift for each differential output
- Frame trigger output
- Error injection capabilities
- Controlled by intuitive graphical user interface SHF Control Center
- Remote control over Ethernet
- Clock distribution for trigger signals and DUTs
- Jitter transparent output signals

Applications

The SHF 12106 A is the ideal pattern source for many R&D or production applications which require high speed test data streams for electrical/optical components or transmission systems. The flexible channel configurations, the wide gap-free data rate coverage and the advanced features make this BPG the perfect fit for

- single channel applications,
  e.g., Fiber Channel®, PCI Express, Serial ATA
- multi-channel applications,
  e.g., 100GbE (using 4x32G DP-QPSK)
- multi-level[1] multi-channel applications using 2 synchronized generators or
  e.g., for 400GbE, 800GbE & 1.6TbE DWDM (e.g., using DP-16QAM or PAM4)
- AWG applications
  the SHF 12106 A + DAC combination is a full "remote head" non-interleaved AWG (Arbitrary Waveform Generator) at a speed of up to 64 GSamples/s

Configurations

The SHF 12106 A can be equipped in a variety of different configurations.

Single 64	– One differential output from 6 to 64 Gbps (two single-ended outputs in total)
Dual 64	– Two differential outputs from 6 to 64 Gbps (four single-ended outputs in total)
Triple 64	– Three differential outputs from 6 to 64 Gbps (six single-ended outputs in total)
Quad 64	– Four differential outputs from 6 to 64 Gbps (eight single-ended outputs in total)

Options

Option Extender SHF C603 B

Two output channels can be multiplexed externally to a data stream up to 120 Gbps by use of a SHF C603 B 2:1 multiplexer. For details please be referred to the data sheet of the SHF C603 B.

Option Extender SHF C911 A

Operating the SHF 12106 A together with SHF C911 A will make the system a 60 GSa/s Arbitrary Waveform Generator (AWG). The vertical resolution is depending on the number of BPG outputs and DAC inputs bits. Example applications include PAM4 with pre-emphasis. For details, please refer to the data sheet of the DACs and the chapters AWG & User-Defined Waveform Capabilities and PAM4 Mode in this document.

Option Extender SHF 616 C

Four output channels can be multiplexed and combined externally to a PAM4 data stream up to 128 GBaud by use of a SHF 616 C. For details please be referred to the data sheet of the SHF 616 C.

[1] up to 16 level signals can be generated with the help of one of SHF's external DAC modules.

Block Diagram

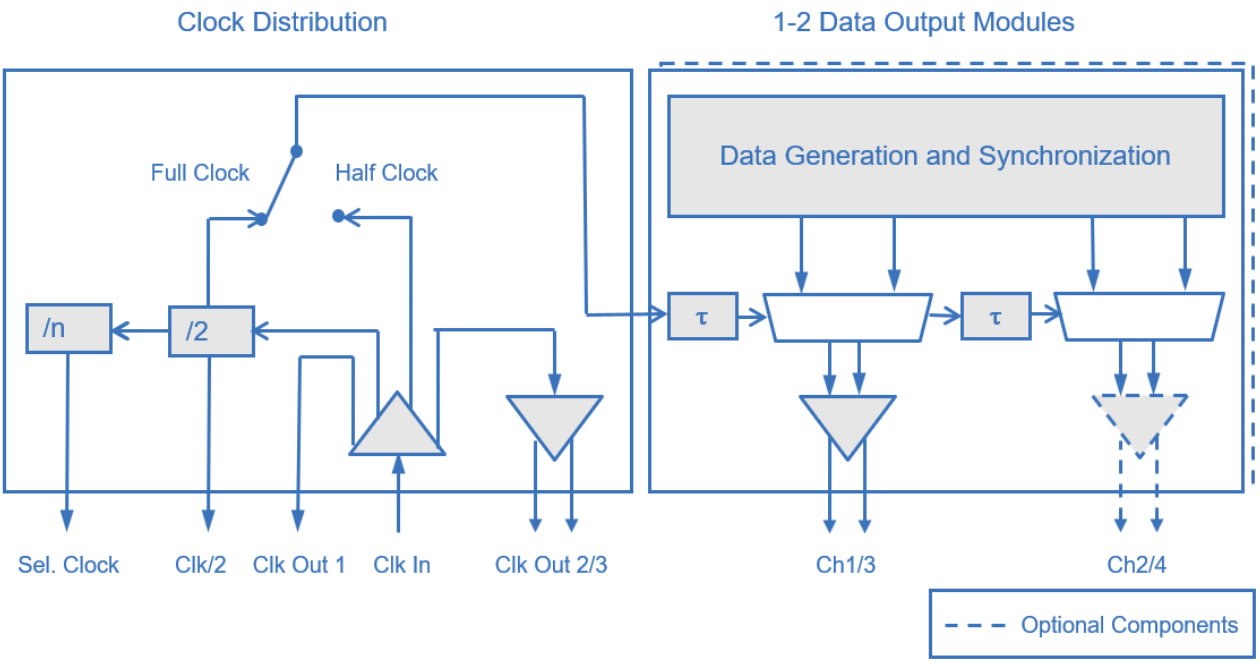


Figure 1 - Block diagram of the SHF 12106 A

The pattern generator consists of up to eight 32 Gbps pattern generation blocks which are synchronized to each other. Four outputs of the pattern generation blocks are 2:1 multiplexed to generate one 64 Gbps data output steam. Each data output module includes two data output channels consisting of a delay line for skew control and a 2:1 MUX.

The clock distribution section processes the incoming clock signal to generate the clock out, clock/2 out and selectable clock out signals. To enable full clock operation, the incoming clock is divided by 2 by selecting full clock mode in the software.

Specifications

Absolute Maximum Ratings

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Clock Input Voltage	mV	$V_{clk\ in}$			900	Peak-to-Peak
External DC Voltage on RF Clock Input Port	V	V_{DCin}	-10		+10	AC coupled input
External DC Voltage on RF Clock Output Ports	V	V_{DCin}	-10		+10	AC coupled outputs
External DC Voltage on RF Data Output Ports	V	V_{DCin}	none[2]		none	DC coupled outputs

2 DC-coupled RF data outputs must not be charged by an external DC voltage

Data Output Specifications

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Minimum Bit Rate	Gbps			2	6[3]	
Maximum Bit Rate	Gbps		64	65		
Maximum Output Level	mV	V_{out}	700 1400	800 1600	900 1800	Single ended Differential Eye amplitude; Adjustable by up to -6 dB; DC coupled ground referenced CML interface
Output DC Level	mv	V_{DCOut}	-400	-500	-600	@ 50 Ω load; constant when adjusting output amplitude
Jitter (RMS) on scope display[4]	fs	J_{RMS}		450	650	
Jitter (RMS) deconvolved[5]	fs	J_{RMS}		403	619	
Jitter (PP)	ps	J_{PP}		2.7	4	
Rise/Fall Time on scope display[6]	ps	t_r/t_f		7	10	20%...80%
Rise/Fall Time deconvolved[7]	ps	t_r/t_f		6	9.3	20%...80%
Crossing	%		46	50	55	
Duty Cycle	%			50		of two consecutive eyes; software adjustable
Skew Control	ps		-25		+25	adjustable in 0.1 ps-steps
Inter-Channel Skew	ps				3	at 64 Gbps with skew control set to 0 ps
Connector Type	Ω			50		1.85 mm (V); female connector

[3] By use of the “Bitrate Divider” – function the minimum output bit rate can be reduced further down to 3 Gbps (see page 14)
[4] Measured with a 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1
[5] Calculation based on typical jitter from oscilloscope data sheet: $J_{RMS\ deconvolved} = \sqrt{(J_{RMS\ measured})^2 - (J_{RMS\ oscilloscope})^2} = \sqrt{(J_{RMS\ measured})^2 - (200\ fs)^2}$
[6] Measured with a 70 GHz sampling head and precision time base triggered by Clk or Clk/2 output, using PRBS 2^{31}-1
[7] Calculation based on typical rise/fall times from oscilloscope data sheet: $t_{r\ deconvolved} = \sqrt{(t_{r\ measured})^2 - (t_{r\ oscilloscope})^2} = \sqrt{(t_{r\ meas.})^2 - (3.68\ ps)^2}$

Clock Specifications

Parameter	Unit	Symbol	Min	Typ	Max	Comment
Clock Input Clock Output 1-3 Clock/2 Output Selectable Clock Output	Ω			50		Connector Type: 1.85 mm (V) female connector 1.85 mm (V) female connector 2.92 mm (K) female connector 2.92 mm (K) female connector
Minimum Clock Input Frequency	GHz	f_{in_clock}			3 6	half clock mode[8] full clock mode[8]
Maximum Clock Input Frequency	GHz	f_{in_clock}	32 64			half clock mode[8] full clock mode[8]
Input Level	mV_{pp}	V_{in_clock}	630		900	AC coupled
Output Level Clock Output 1-3 Clock/2 Output Selectable Clock	mV_{pp}	V_{out_clock}	 630 500 300	 800 650 500	 1000 900 700	 AC coupled, @ P_{in}=0 dBm AC coupled AC coupled
Output Frequency Clock Output 1-3 Clock/2 Output Selectable Clock Output	 GHz GHz GHz	f_{out_clock}	 3 1.5 0.023		 64 32 32	 same as input frequency half of input frequency input frequency/N (N= 2, 4, 8, 16, 32, 64, 128)

[8] The operating bit rate is determined by a clock signal from an external clock source which is not part of the pattern generator. The outputs can operate at both full clock and half clock, so e.g., a 20 GHz or a 40 GHz signal is required for 40 Gbps operation.

General Specifications

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Weight	kg	m			12	Fully Equipped
Dimensions	mm	WxDxH				340x480x146
Operating Temperature	°C	T_{OP}	10		35	
Storage Temperature	°C	T_{ST}	-20		70	@ 95 % RH max.
Working Humidity	%		20		90	Non condensing

Rear Panel Connections

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Power Supply	V	U		48		48 V switching power supply is included
Power Consumption	W	P			120	Max. Configuration @48 V
Power Supply Connector						4 Pin Power DIN
Common Ground Connector						4 mm socket
Network Connectors						RJ-45 Ethernet
USB Connectors						For future use

Front Panel Connections

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
Auxiliary Power Output	V	U		–5 +5 +12		Max. 1.5 A Max. 1.5 A Max. 1.5 A
Auxiliary Power Connector						Lemo EPG.OB.304.HLN
Common Ground Connector						4 mm socket
Network Connector						RJ-45 Ethernet
USB Connectors						For future use

Patterns

Pattern	Polynomial	Reference
PRBS 2^7-1	$G(x) = 1 + x^6 + x^7$	
PRBS 2^9-1	$G(x) = 1 + x^5 + x^9$	ITU-T O.150 5.1 IEEE 802.3 68.6.1
PRBS 2^{10}-1	$G(x) = 1 + x^7 + x^{10}$	
PRBS 2^{11}-1	$G(x) = 1 + x^9 + x^{11}$	ITU-T O.150 5.2
PRBS 2^{13}-1	$G(x) = 1 + x + x^2 + x^{12} + x^{13}$	IEEE 802.3 94.3.10.8
PRBS 2^{15}-1	$G(x) = 1 + x^{14} + x^{15}$	ITU-T O.150 5.3
PRBS 2^{20}-1	$G(x) = 1 + x^3 + x^{20}$	
PRBS 2^{23}-1	$G(x) = 1 + x^{18} + x^{23}$	ITU-T O.150 5.6
PRBS 2^{31}-1	$G(x) = 1 + x^{28} + x^{31}$	ITU-T O.150 5.8 IEEE 802.3 49.2.8

User Pattern Capabilities

Parameter	Unit	Symbol	Min	Typ	Max	Conditions
User Pattern Memory size		Gbit			16	Per channel
User Pattern Granularity		Bit		256		For more details see Chapter User Pattern Capabilities

Example Patterns Provided

Pattern	Polynomial
SSPR[9]	OIF-CEI-03.1 Annex 2.D.2
JP03A[9]	IEEE 802.3 94.2.9.1
JP03B[9]	IEEE 802.3 94.2.9.2
QPRBS13[9]	IEEE 802.3 94.2.9.3
Transmitter Linearity[9]	IEEE 802.3 94.2.9.4
PRBS13Q[9]	IEEE 802.3 120.5.11.2.1
SSPRQ[9]	IEEE 802.3 120.5.11.2.3
Square Wave Quaternary[9]	IEEE 802.3 120.5.11.2.4

[9] Is a PAM4 pattern and can be generated by combining the BPG output signals with a DAC

Output Adjustment Capabilities

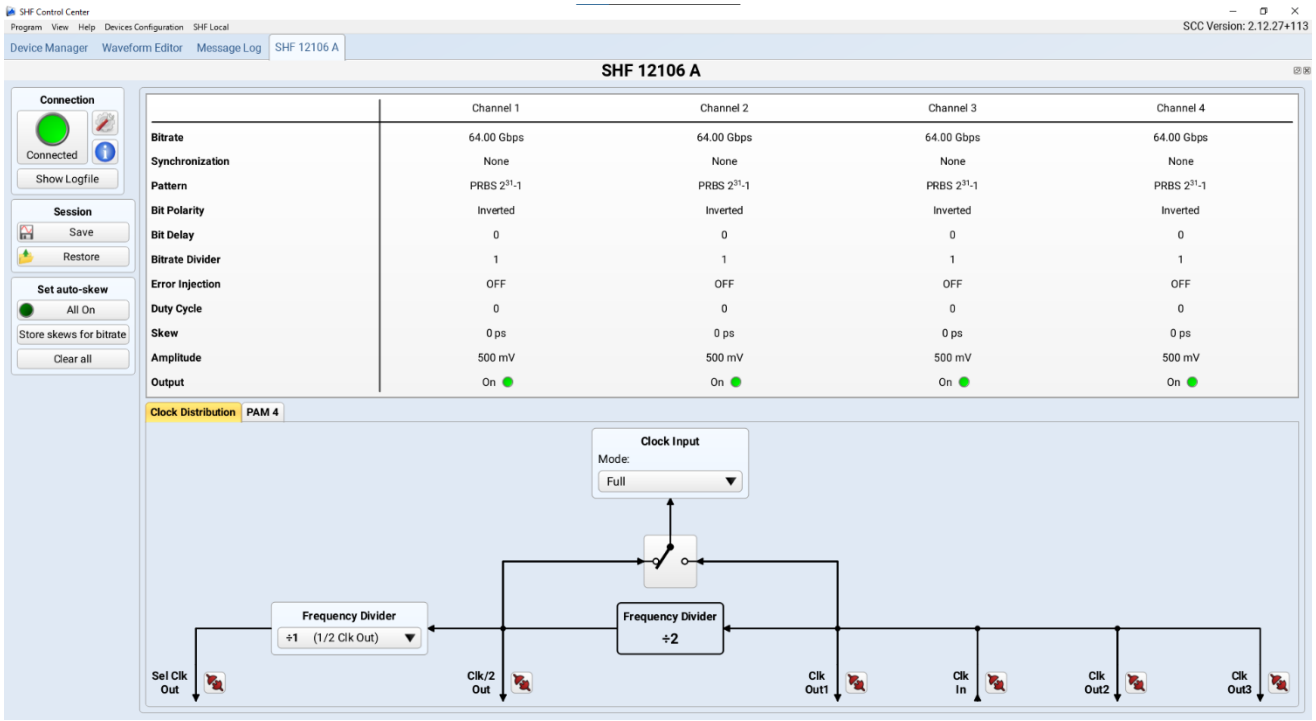


Figure 2 - SHF Control Center window for the SHF 12106 A

Bit Rate

The bit rate of all outputs is continuously adjustable by a single external clock signal.

Clock Input

In full clock mode, the BPG will need a 64 GHz clock signal to generate a 64 Gbps data signal. In half clock mode, a 32 GHz clock signal will be needed to generate a 64 Gbps data signal. Internally the SHF 12106 A operates in half clock mode. When selecting full clock mode, a divider is used to generate the half clock needed internally from the externally provided full clock.

Selectable Clock

The selectable clock output provides a divided clock signal derived from the clock input signal. A divider ratio of 1/n with n = 2, 4, 8, 16, 32, 64 or 128 can be selected.

AUX Power

This control is needed to enable the aux power voltages provided on the front panel.

Group Synchronization

The data outputs can be grouped. All data outputs of one group are bit synchronized to enable AWG functionality together with a DAC, cross talk measurements and PRBS conformed multiplexing.

Pattern Type

Pre-defined PRBS patterns from 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{13}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1 and 2^{31}-1 are available. User-defined binary patterns can be loaded from file in single column text file format. All PRBS and user patterns can be assigned individually to each channel.

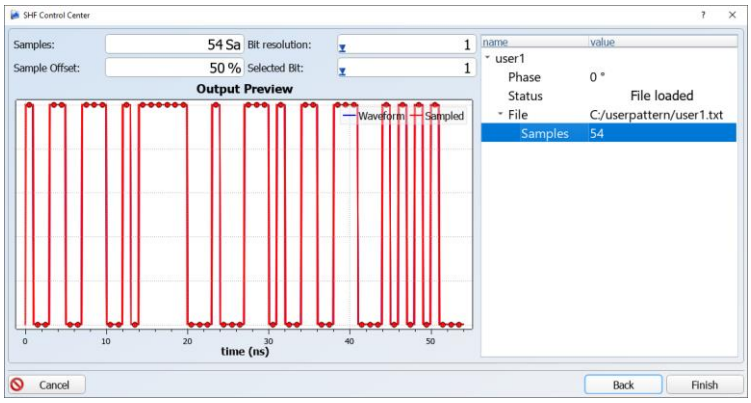


Figure 3 - SHF Control Center upload GUI for binary user patterns

Pattern Polarity

All patterns can be inverted by use of this function.

Bit Delay / Bit Shift

In case two or more PRBS patterns of the same length are selected it is possible to control the starting point of each bit sequence (in 1 bit steps up to the total PRBS length).

Bit Rate Divider

The 'bit rate divider' is a software function to transmit the same bit two times and thus reduces the data rate (divided by 2).

Error Injection

For testing purposes, a fixed error rate can be added to the date stream.

Duty Cycle

The duty cycle of two consecutive eyes/bits is automatically set to 50 %. However, in case the application requires a modification or a further optimization, this could be done with a few clicks.

Skew

The timing of every output channel can be adjusted individually in 0.1 ps steps (please see chapter Skew Control Function for more details).

Amplitude

The output amplitude of each channel is adjustable independently.

Output On/Off

The outputs can be turned on and of individually. During and after start up these are turned off to prevent any damage to the DUTs attached.

AWG & User-Defined Waveform Capabilities

The SHF 12106 A and a SHF DAC are not just two discrete modules connected together as the SHF Control Center software (SCC) unifies them to virtually one AWG device.

The SCC offers an interface for user defined signals by use of the Python programming language or the user may load externally generated signals from software like MATLAB. A set of commonly used signals is provided with the SHF Control Center. The software only needs to know which BPG output is physically connected to which DAC input. The SHF Control Center will calculate the user pattern for each channel in a way that the DAC generates the desired arbitrary signal.

The best results are achieved with the SHF C911 A 4-Bit DAC and a SHF 12106 A with at least 4 channels as this architecture provides a vertical resolution of 2^4=16 steps reducing quantization errors.

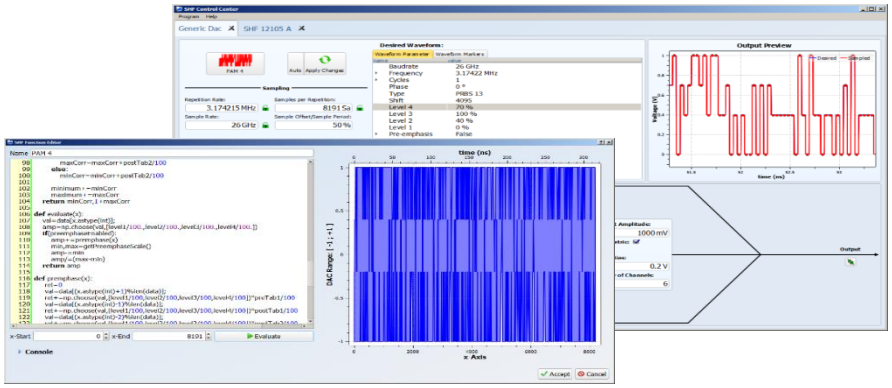


Figure 4 – Arbitrary Waveform Generator Interface

The SHF 12106 A has a built-in 16 Gbit user pattern memory for each output channel. Due to the memory width of 256 bits, there is a granularity requirement of 256 bits which can be overcome by repeating the pattern until the least common multiple of the pattern length and 256 is met.

The SHF Control Center software supports creating, editing and converting different formats of user pattern files. For example, it will repeat automatically user patterns not fulfilling the granularity requirement until the granularity of 256 is met. For patterns up to 64 Mbit this is always possible. Patterns larger than 64 Mbit have to fulfill the following prerequisites:

Pattern length up to	Pattern length has to be a multiple of
64 Mbit	1
128 Mbit	2
256 Mbit	4
512 Mbit	8
1 Mbit	16
2 Gbit	32
4 Gbit	64
8 Gbit	128
16 Gbit	256

Two BPG output channels (1&3, 2&4) share a common memory controller, so that their patterns need to be of the same length or need to be repeated until the least common multiple is met. For most applications such as PAM, AWG, DACs and Muxes the patterns need to be of the same length anyway.

PAM4 Mode

For binary data a BPG has obvious advantages over an AWG because the bit/baud rate always equals the sample rate (no fractional oversampling) and because logical pattern generation techniques can be applied without utilizing a rather slow and small memory. With the SHF 12106 A these advantages do also apply to a BPG/DAC combination when generating PAM4 signals where even the individual eye heights or pre-emphasis can be achieved and adjusted on the fly without waiting for the memory to be loaded and by still transmitting very long patterns (e.g., PRBS 2^{31}-1 or PRBS31Q).

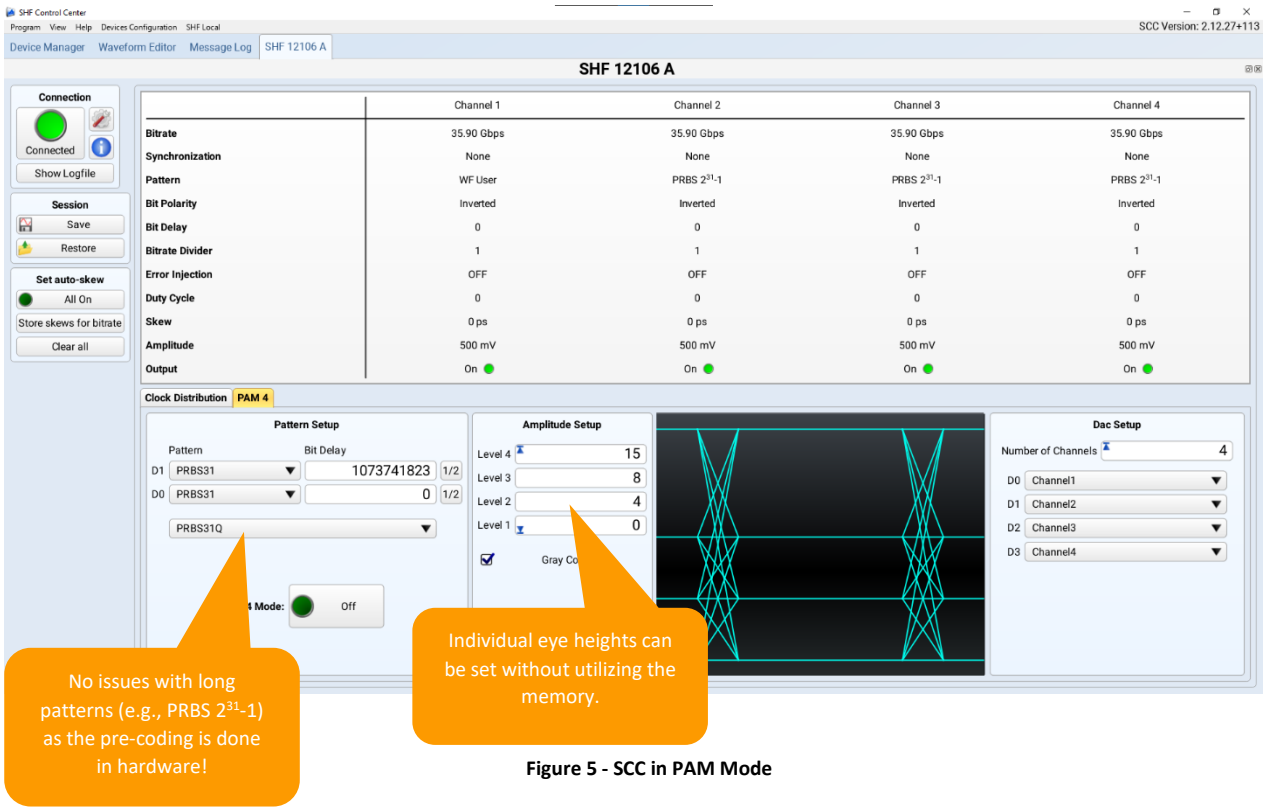


Figure 5 - SCC in PAM Mode

Jitter Transparency

By modulating the clock input signal with a low frequency signal, one can quickly and easily create jittered clock signals with complex properties to emulate jittered high speed NRZ data (Fig.8). Adding a DAC gives the possibility to generate jittered PAM signals (Fig. 9 & 10). For more information see Application Note “Creating Complex Jittered Test Patterns” on SHFs web page.

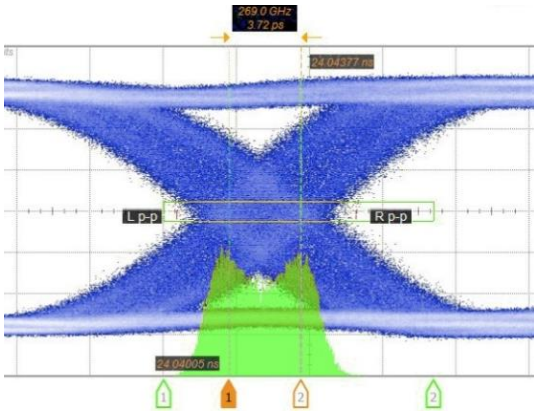


Figure 6 – Sine-jittered data output signal from SHF 12106 A

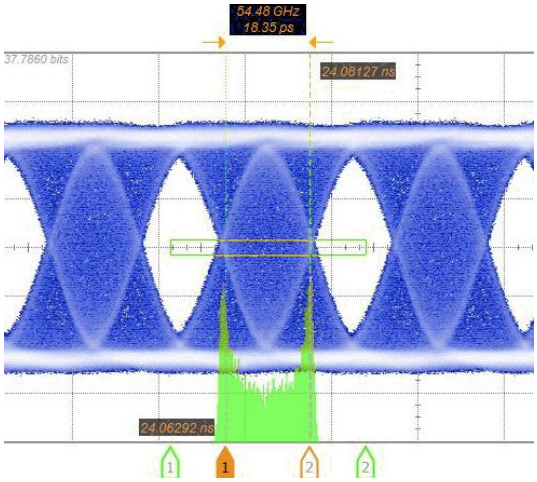


Figure 7 – Sine-jittered data output signal (MSB) from a SHF DAC

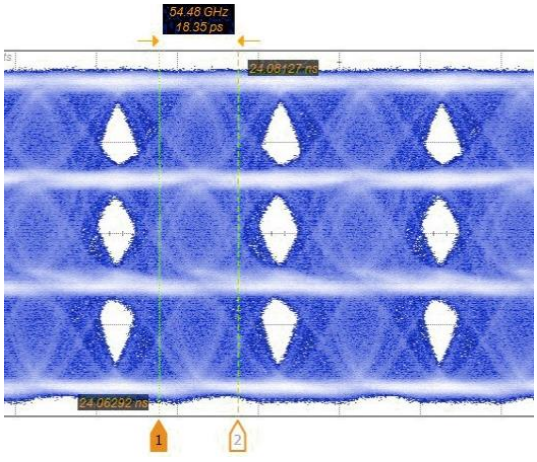


Figure 8 – Sine-jittered data output signal (PAM4) from a SHF DAC

Skew Control and Bit Delay Functions

The skew control and bit delay functions allow the channel timing to be adjusted relative to each other. As a result, timing delays between individual output channels can be tuned in 0.1 ps steps (using skew control), as well as over many integer bit periods (using the bit delay function). The figures below show the SHF Control Center with this feature and an example of delay between two channels for skew within a bit and more than one bit.

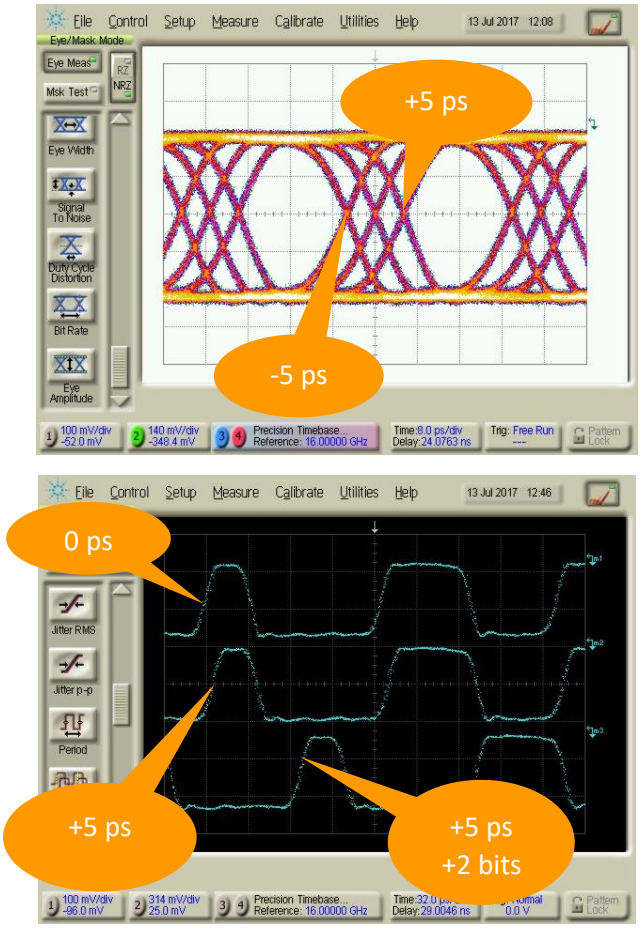


Figure 9 – Skew control & integer bit delay

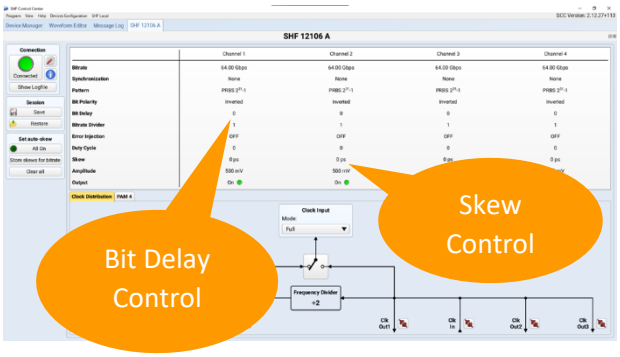
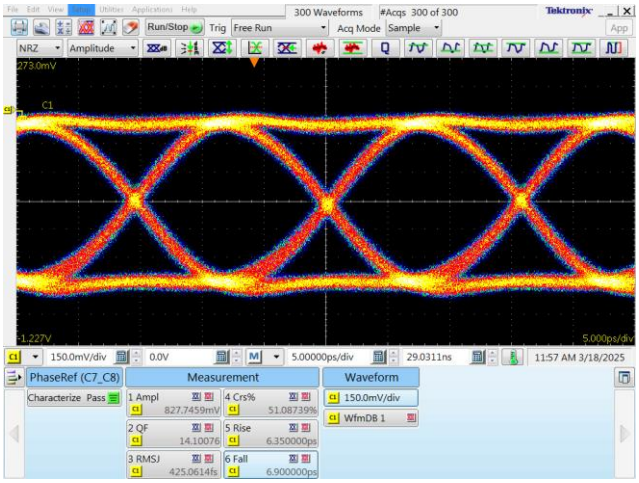


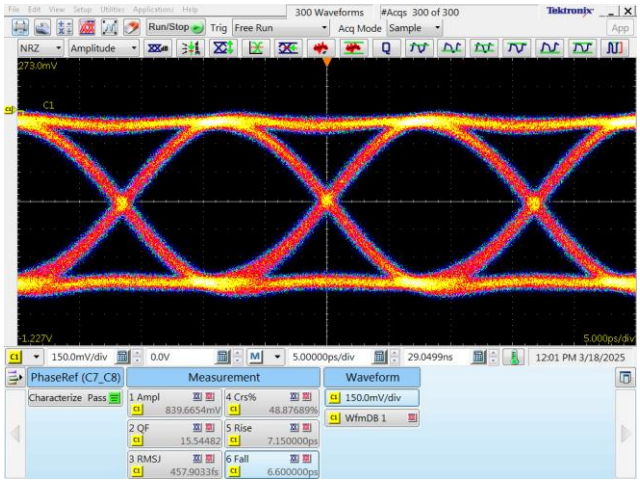
Figure 10 – Bit delay and skew control software representation

Typical Output Waveforms

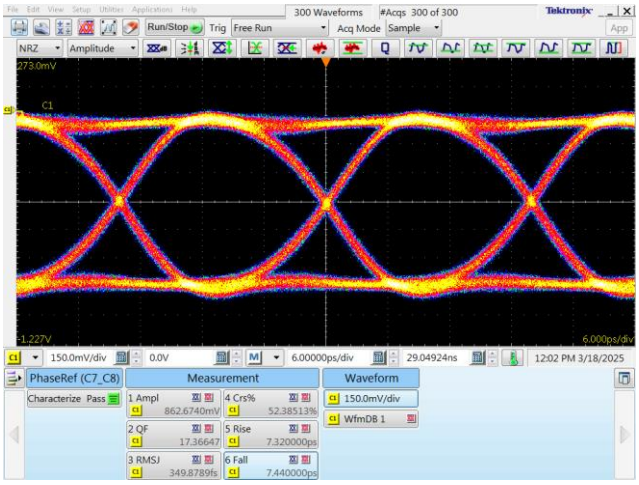
Data Output Signals



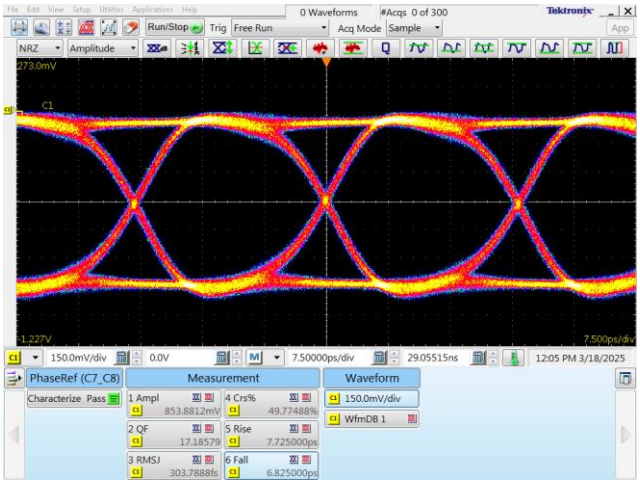
64 Gbps output at maximum output level



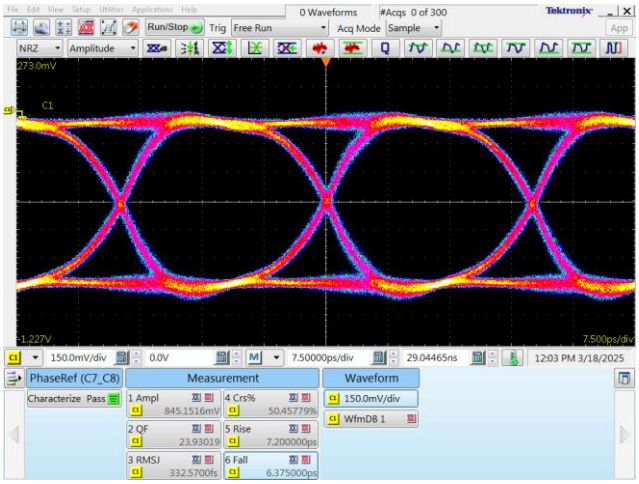
60 Gbps output at maximum output level



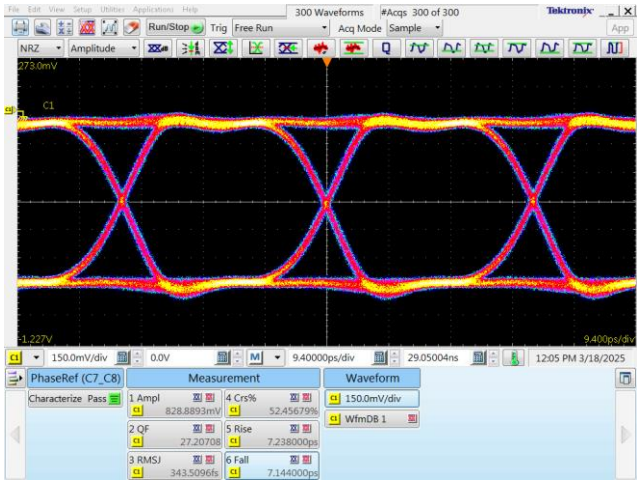
50 Gbps output at maximum output level



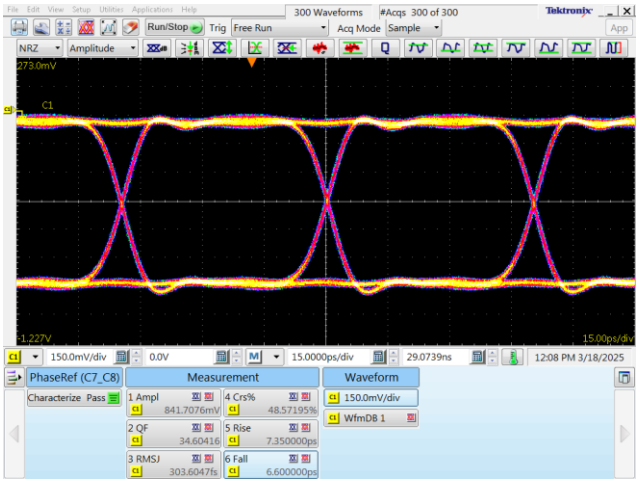
43 Gbps output at maximum output level



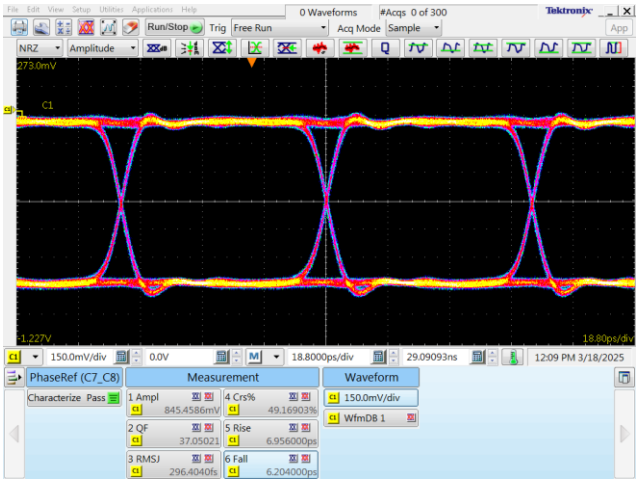
40 Gbps output at maximum output level



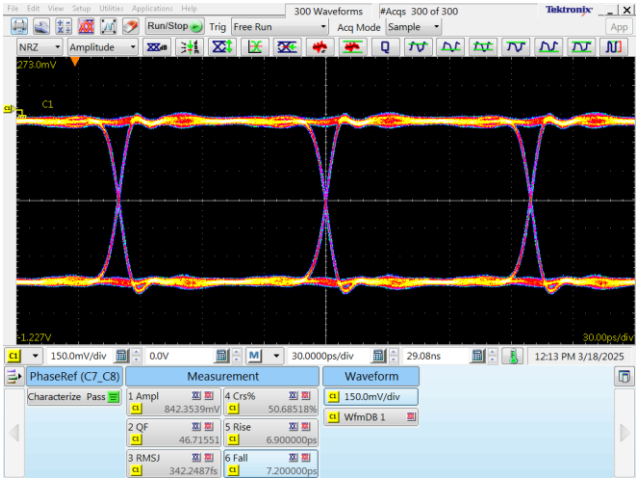
32 Gbps output at maximum output level



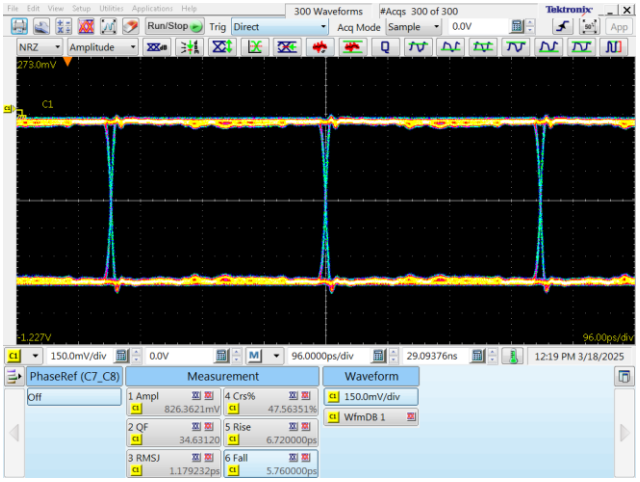
20 Gbps output at maximum output level



16 Gbps output at maximum output level

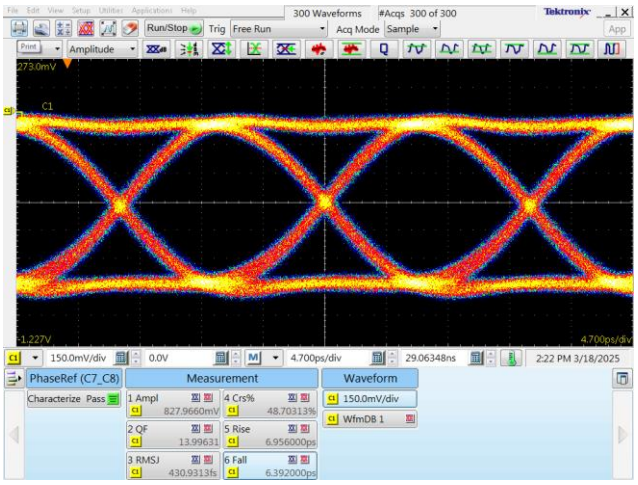


10 Gbps output at maximum output level

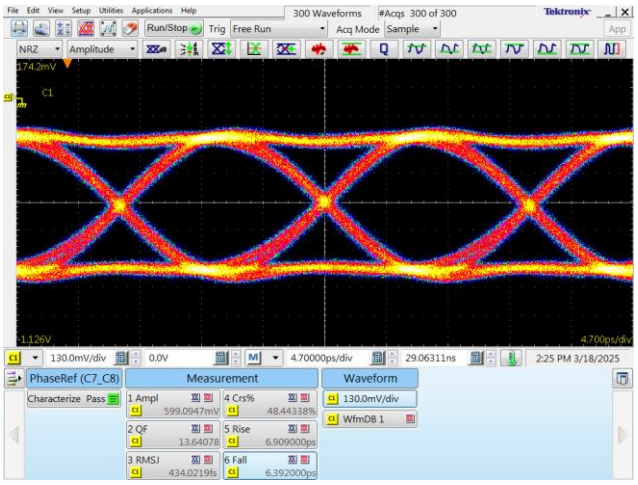


3 Gbps output at maximum output level

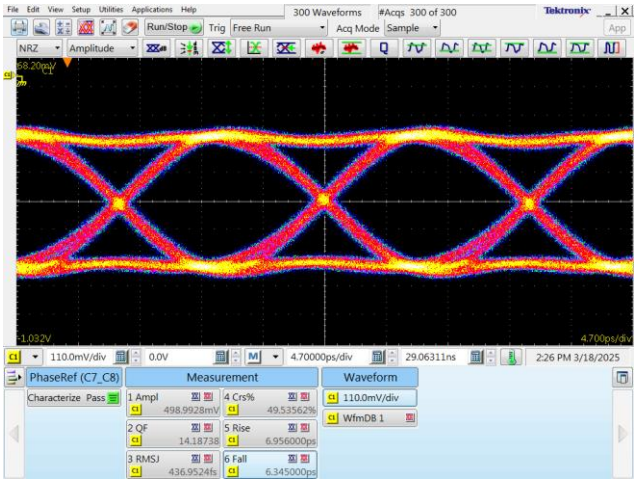
Data Output Signals - Amplitude Adjustment



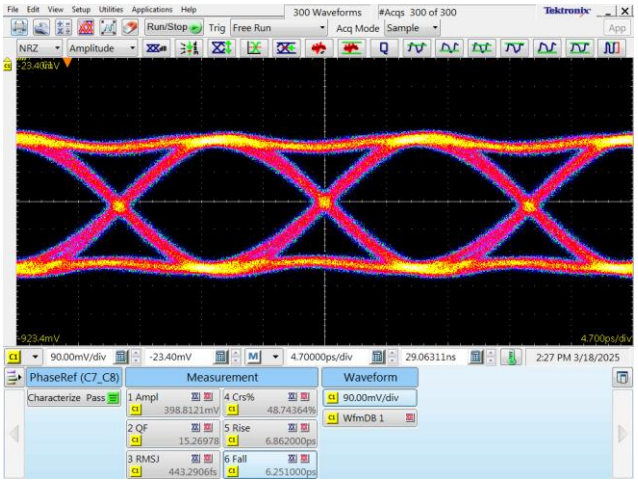
64 Gbps output at 830 mV



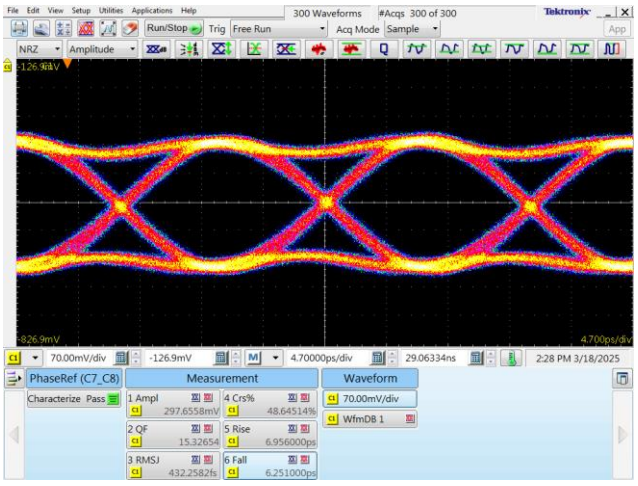
64 Gbps output at 600 mV



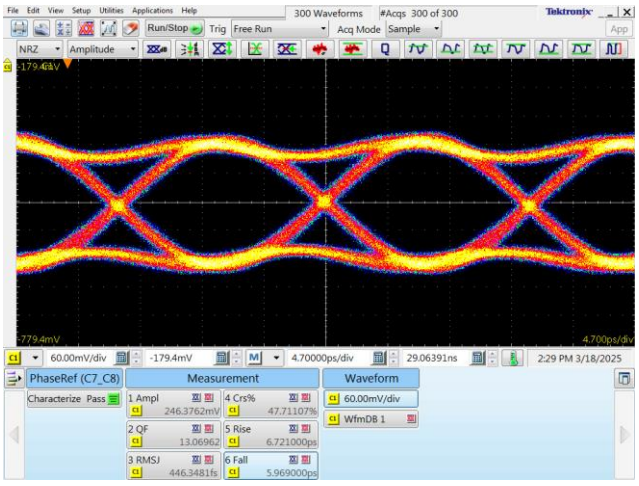
64 Gbps output at 500 mV



64 Gbps output at 400 mV

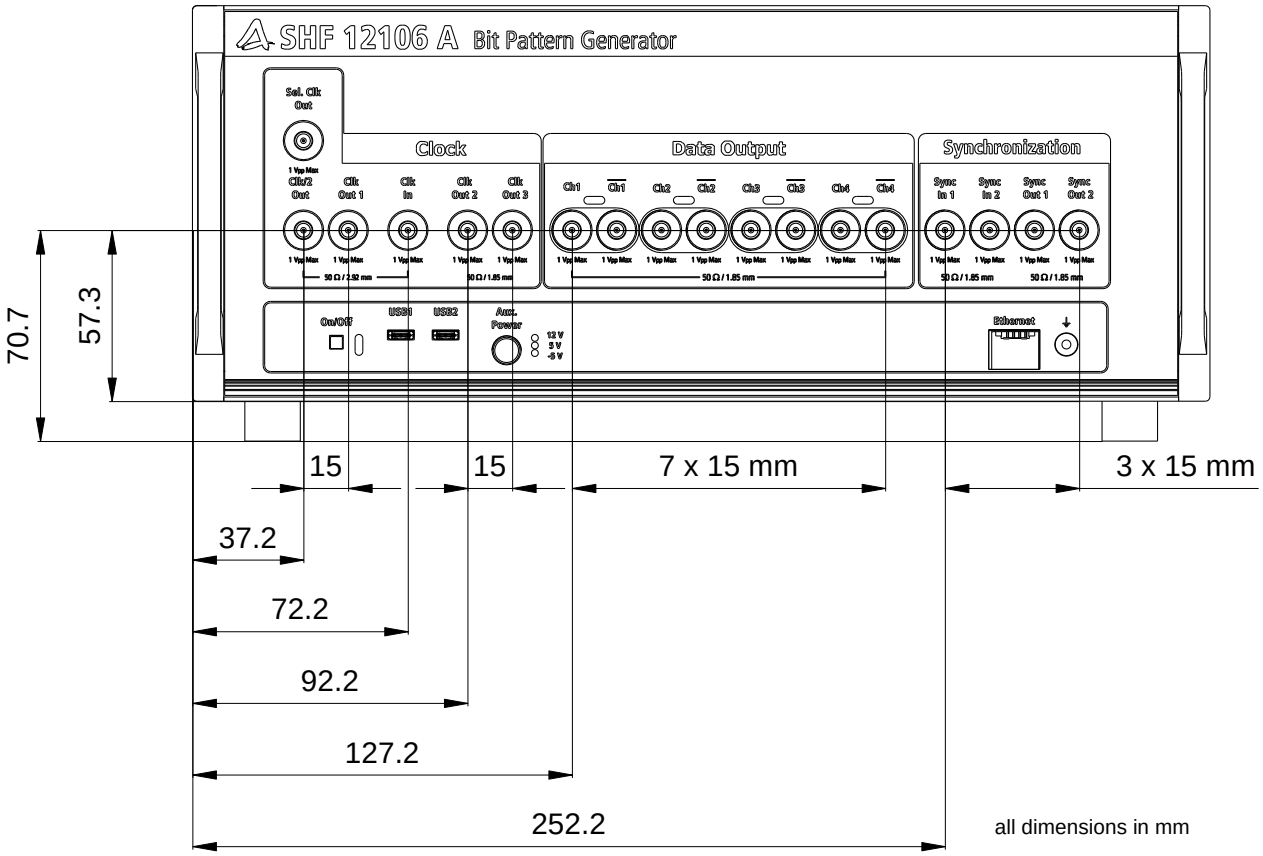


64 Gbps output at 300 mV

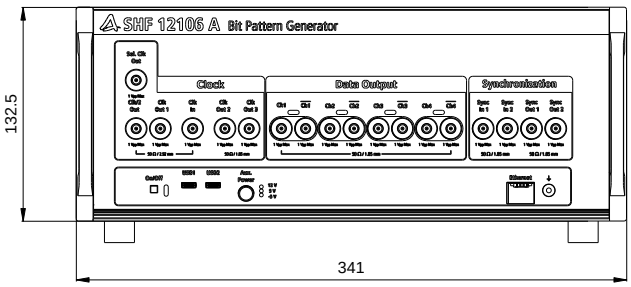


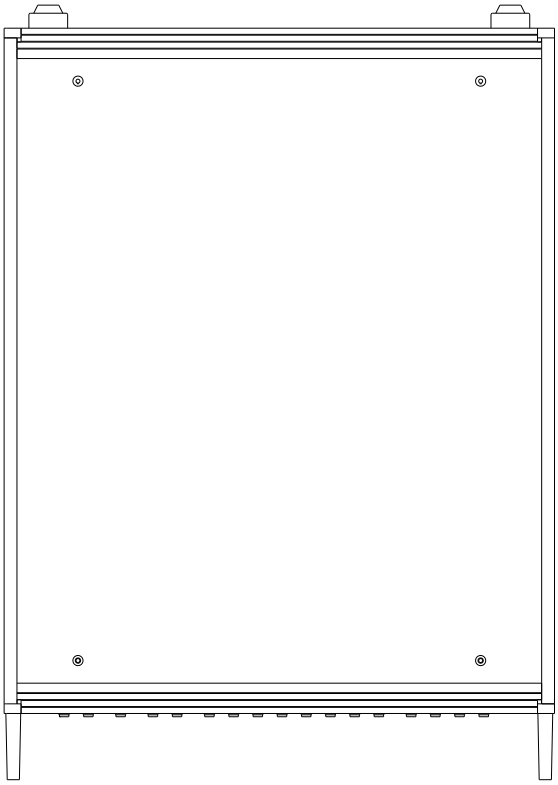
64 Gbps output at 250 mV

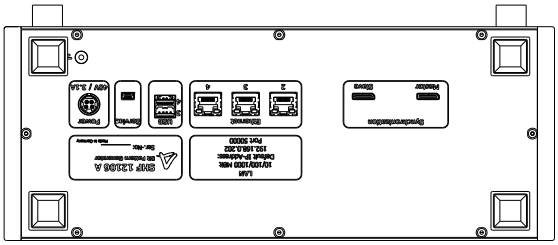
Outline Drawing – Front Panel

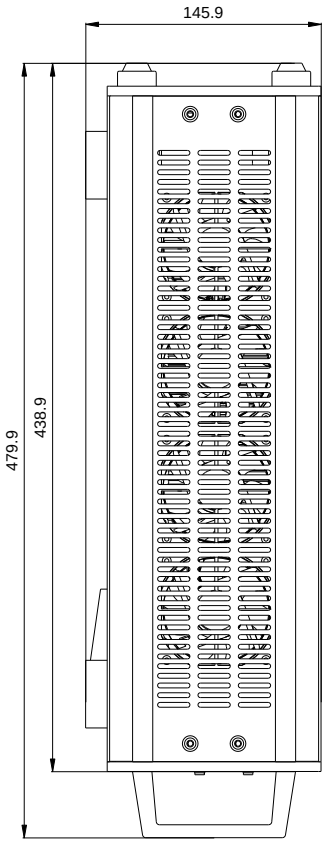


Outline Drawing - Case



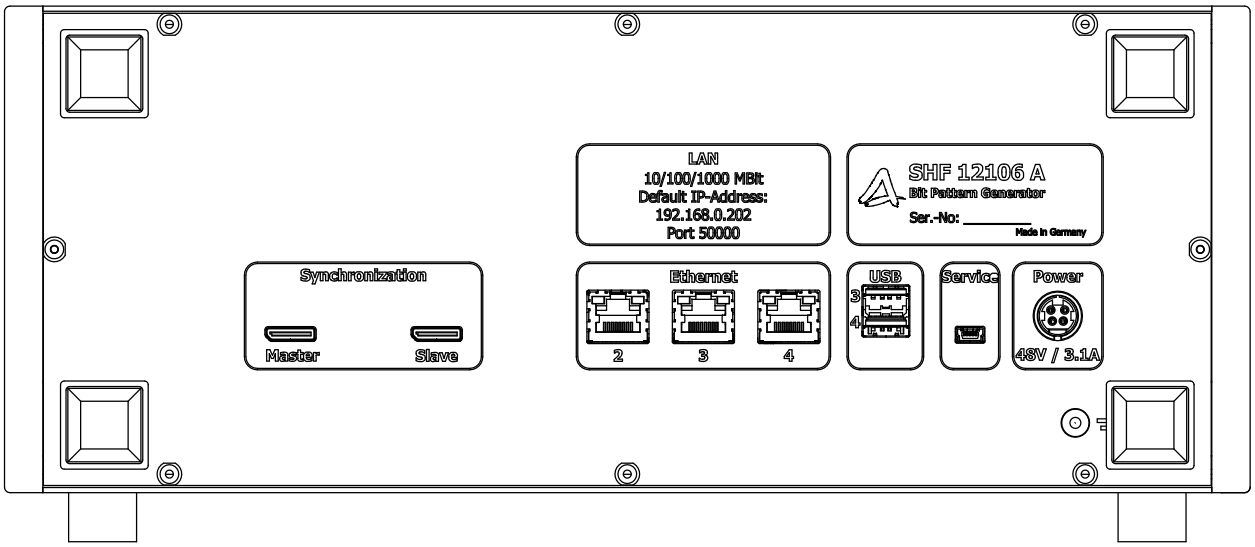






all dimensions in mm

Outline Drawing – Back Panel



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