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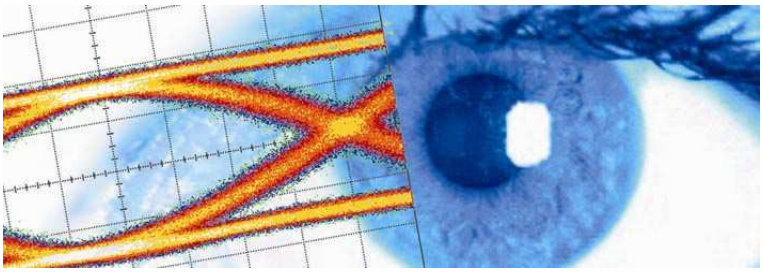


Datasheet
SHF 19120 A

2.85 GSa/s Arbitrary Waveform Generator with 4x 10.3125 Gbps BPG Outputs

For illustration only, actual product may vary

Description

The SHF 19120 A is a 2.85 GSa/s, 14 bit Arbitrary Waveform Generator with four 10.3125 Gbps bit pattern outputs. Its high AWG bandwidth (>1.2 GHz), high output amplitude (1.2 V on DC output, +8.2 dBm on the AC output) and large sample memory size (1 Giga Sample) make it a versatile arbitrary generator.

Three outputs (Direct, DC and AC) cover a wide range of test scenarios (jitter, glitched signal, modulation and modulated signal generation, etc).

Two markers with a 2-sample resolution can be used to trigger external equipment. Two edge/level trigger inputs start or pause the signal generation.

Two or more SHF 19120 A instruments can be synchronized together via their 10 MHz references.

A sample sequencer allows the creation of complex waveforms with memory-saving repeated patterns (to be enabled in the future with a software update).

In addition to the three analog outputs, the SHF 19120 A can generate up to four 10.3125 Gbps PRBS signals with pre-emphasis on the rear panel, driven by the DAC clock, or by an external clock.

The SHF Control Center software allows a complete control of the SHF 19120 A, including a waveform editor with a waveform library and an equation editor. When connecting a keyboard, a mouse and a monitor, the SHF 19120 A can be controlled without a computer, via the embedded version of the SHF Control Center.

SHF 19120 A : actual waveform and GUI

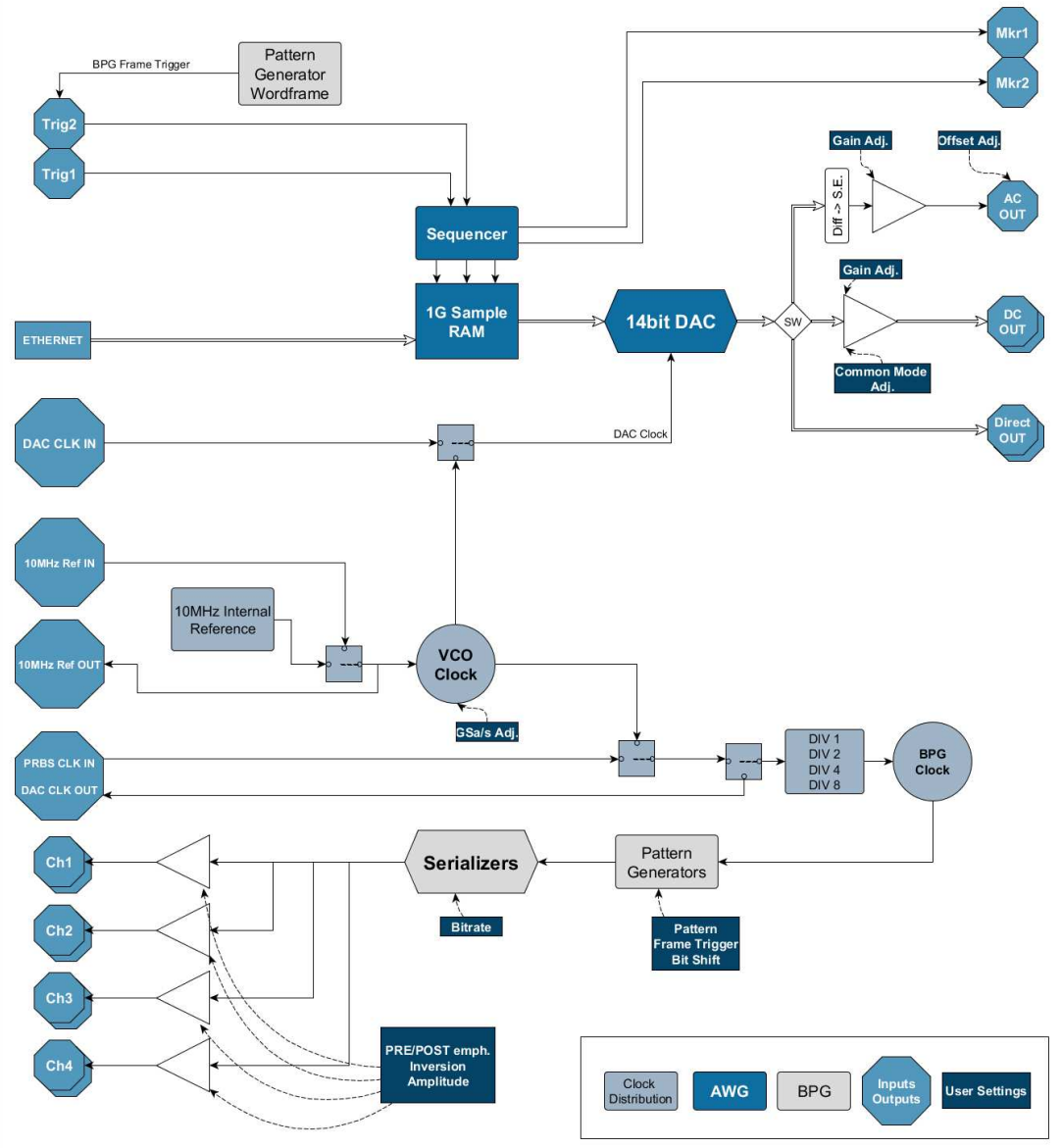
Features

- Arbitrary Waveform Generator
  - Sampling frequency f_{DAC} up to 2.85 GHz
  - 1 GSa – sample memory
  - Three types of outputs: Direct, DC coupled (1.2 V_{pp}) and AC coupled (+8 dBm max, in 0.1 dB steps)
  - High output bandwidth: DC to 1.2 GHz for the direct and DC outputs, 20 MHz to 500 MHz for the AC output
  - Up-sampling: Double Interpolation Mode, the signal spectrum is shifted to f_{DAC}, doubling the effective DAC update rate
  - Two sample-synchronous marker outputs
  - Two sample-synchronous trigger (edge/level) inputs
  - Output skew control in combination with triggers and markers delays help the synchronization of several SHF 19120 A AWGs
  - Outputs and inputs for the DAC clock and the 10 MHz reference
- Bit Pattern Generator
  - Four PRBS differential outputs with lane bitrates from 1 Gbps to 10.3125 Gbps (with the possibility of overclocking to 12.5 Gbps)
  - Nine PRBS patterns (from $PRBS^{7}$-1 to $PRBS^{31}$-1), plus two square wave patterns of half line rate (SQUARE2) and line rate ÷ 32 (SQUARE32).
  - Frame trigger output
  - Bit skew adjustment
  - Pre and post cursor pre-emphasis
- Computer controlled via a 1 G Ethernet link or
- Stand-alone operation, with keyboard, mouse and monitor
- Modern and user-friendly software

Applications

- Jitter source
- Development of Test and Measure Equipment
- Wideband signals
- Wireless communications
- Radar signals
- Multilevel signals
- High speed serial link testing
- Backplane characterization

Block Diagram



Absolute Maximal Ratings

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Power Supply Voltage	V				13	
Trigger Inputs	V				2.5	
DAC Clock Input	dBm				3	
PRBS Clock Input	dBm				3	
10 MHz Input	V				3	Peak-to-Peak

Specifications – SHF 19120 A

Unless specified, all measurements are taken with f_{DAC} = 2.85 GHz, single-ended.

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
General characteristics - AWG						
Resolution	bits			14		Markers do not decrease the resolution or memory size.
Sample Rate	GSa/s	f_{DAC}	1.4		2.85	
RF Connectors				SMA		
Output Adjustable Delay	Sample Clock Periods		0		254	
Output Adjustable Delay Step	Sample Clock periods		2			
General characteristics - BPG						
Channels				4		
Bit Rate	Gbps		0.372		10.3125	Overclocking up to 12.5 Gbps possible. See bit rate ranges, page 12
RF Connectors				SMA		Differential
External Clock Input Multiplier Factor			1		8	The BPG bitrate will be the external clock frequency multiplied by this factor
Adjustable Delay Length	bit		0		127	With a 1 bit step

Direct Output

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Impedance	Ohm			50		
Voltage Window Minimum	mV		65		75	Single-ended. Includes the output offset from internal biasing
Voltage Window Maximum	mV		800		810	Single-ended. Includes the output offset from internal biasing
Adjustable Full-Scale Amplitude Minimum	mV		220		225	Single-ended, Peak-to-Peak
Adjustable Full-Scale Amplitude Maximum	mV		720		725	Single-ended, Peak-to-Peak
Full-Scale Amplitude Step	mV			5		
Full-Scale Amplitude Accuracy	mV			±50		
Random Jitter RMS	ps			3	5	Measured with PRBS-7, sample clock for trigger.
Rise/Fall Time	ps				110	0.7V, 1.425 GHz square signal, from 20% to 80%
3dB Bandwidth	GHz		1.2			
Calculated Bandwidth	GHz			3.1		0.35 / Rise time
SFDR *Spurious Free Dynamic Range*	dBc				-38	285 MHz 0 dB Output, harmonics excluded, 40 dB interpolation filter enabled.
Two-Tone IMD *Inter Modulation Distortion*	dBc				59	f_1= 19.9 MHz f_2= 20.1 MHz ; 700 mV_{pp} ; $2f_2$-f_1
Harmonic Distortion					1%	310 MHz Output, 730 mV_{pp} ; 5 first harmonics.

Direct output: Differential or Single-ended output (Unused output must be terminated with a 50 Ω load), DC-coupled.

DC Output						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Impedance	Ohm			50		
Voltage Window Minimum	mV		-100		-200	The signal will be clipped outside the voltage window
Voltage Window Maximum	mV		1200		1400	
Adjustable Full-Scale Amplitude Minimum	mV		250		400	Single-ended, Peak-to-Peak
Adjustable Full-Scale Amplitude Maximum	mV		1200		1400	Single-ended, Peak-to-Peak
Full-Scale Amplitude Step	mV			5		
Full-Scale Amplitude Accuracy	mV			±50	±100	
Adjustable Offset	mV		100		1000	Limited by the output voltage window
Offset Step	mV			5		
Offset Accuracy	mV			±50		
Random Jitter RMS	ps			2	5	Measured with PRBS-7, 0.7 V_{pp}, sample clock for trigger.
Rise/Fall Time	ps				110	Measured with PRBS-7, 0.7 V_{pp}, sample clock for trigger, from 20% to 80%
3dB Bandwidth (from DC)	GHz		1.2			Measured with the 40 dB interpolation filter enabled
Calculated Bandwidth	GHz			3.1		0.35 / Rise time
SFDR *Spurious Free Dynamic Range*	dBc				-60	285 MHz 0 dB Output, harmonics excluded, 40 dB interpolation filter enabled.
Two-Tone IMD *Inter Modulation Distortion*	dBc				-54	f_1= 19.9 MHz f_2= 20.1 MHz ; 700 mV_{pp} ; $2f_2$-f_1
Harmonic Distortion					0.2%	310 MHz Output, 350 mV_{pp}, 400 mV offset ; 5 first harmonics.

DC output: Differential or Single-ended output (Unused output must be terminated with a 50 Ω load), DC-coupled

AC Output						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Impedance	Ohm			50		
Adjustable Full Scale Amplitude Minimum	dBm		-28.2		-28	
Adjustable Full Scale Amplitude Maximum	dBm		8		8.2	
Adjustable Amplitude Step	dB			0.1		
Accuracy	dBm			0.2	0,4	
Adjustable Offset	V		0		4.5	Integrated bias tee
Adjustable Offset Step	mV			50		
Offset Accuracy	mV			±50	±100	
3dB Bandwidth (starting at 20 MHz)	MHz			550		0dB sinus, 40 dB interpolation filter enabled, sweep 20 MHz to 600 MHz
6dB Bandwidth (starting at 20 MHz)	MHz		1425			0dB sinus, 40 dB interpolation filter enabled, sweep 20 MHz to 1425 MHz
SFDR *Spurious Free Dynamic Range*	dBc				-49	275 MHz 0 dB Output, harmonics excluded, 40 dB interpolation filter enabled. DC to $f_{DAC.}$
Two-Tone IMD *Inter Modulation Distortion*	dBc				-56	f_1= 91.8 MHz f_2= 93.6 MHz ; 0 dBm ; $2f_2$-f_1
Harmonic distortion					0.31%	310 MHz Output, 0 dBm ; 5 first harmonics.
Double Interpolation mode						
3dB Bandwidth	MHz			650		-10 dBm Output, 40 dB interpolation filter enabled. f_{DAC}/2. to $f_{DAC.}$
SFDR *Spurious Free Dynamic Range*	dBc				-41	2.75 GHz -10 dBm Output, harmonics and f= 275 MHz excluded, 40 dB interpolation filter enabled. DC to $f_{DAC.}$
Two-Tone IMD *Inter Modulation Distortion*	dBc				-69	f_1= 1.63 GHz f_2= 1.66 GHz ; -10 dBm ; $2f_2$-f_1

AC output: Single-ended output, AC coupled, with adjustable offset

Markers – Two markers outputs – Front panel						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Amplitude	V		2.1	2.5		LVCMOS25
Impedance	Ohm			50		Match to 50 Ohms for best signal.
Resolution	Sample			2*		Sample synchronous
Width	Sample		1		1G	A single marker will be automatically extended to a width of 1ns
Maximum Repeatability	Sa			3		Each marker must have a dead time of 3 samples before the next marker.
Maximum Frequency	MHz			475		With f_{DAC} =2.85 GSa/s
Jitter	ps			500	600	With an even count of samples
Adjustable Delay	Sample Clock periods		0		254	
Adjustable Delay Step	Sample Clock periods			2		

**2 samples position uncertainty when generating a repeating signal with an odd sample count period and a marker on each period. The SHF Control Center will issue a warning when this situation happens.*

Triggers – Two triggers inputs – Front panel						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Type	Rising edge, falling edge, gated high, gated low.					
Amplitude Threshold Low	V	V_{IL}	-0.3		0.7	LVCMOS25
Amplitude Threshold High	V	V_{IH}	1.7		2.8	LVCMOS25
Delay	Sample Clock periods			200		From Trigger in to Signal present on output
Pulse Width	ns		1			
Adjustable Delay	Sample Clock periods		0		126	
Adjustable Delay Step	Sample Clock periods			2		

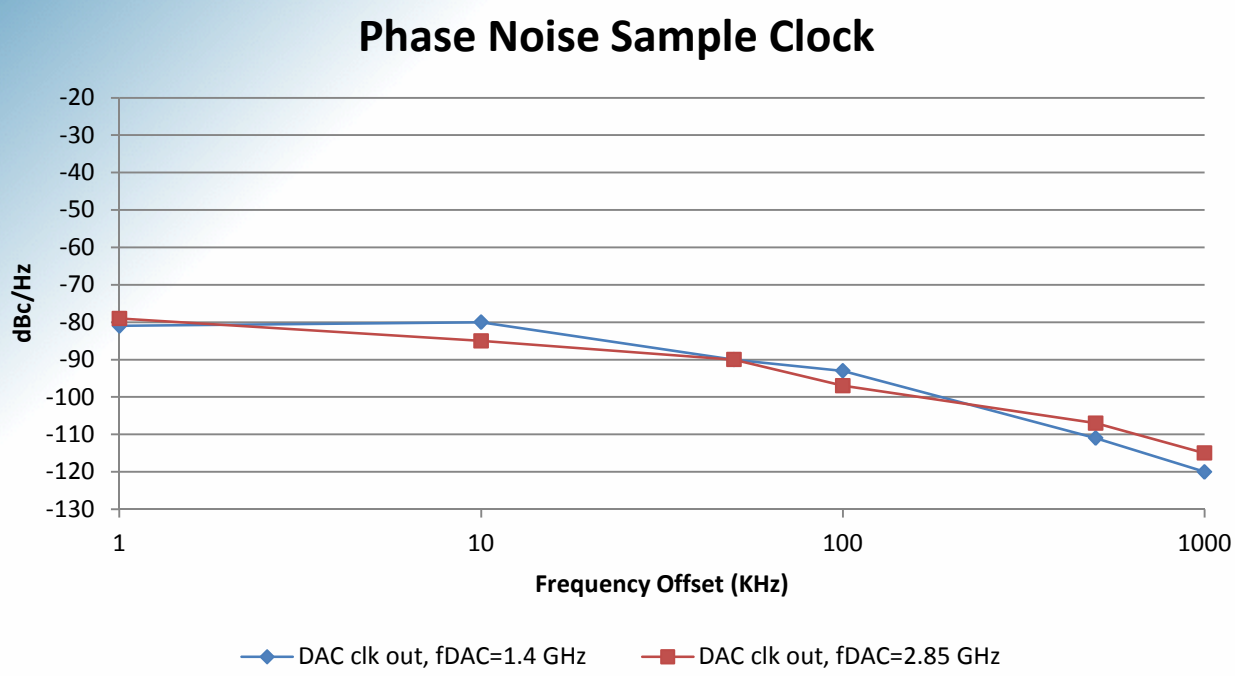
Internal reference						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Frequency	MHz			10		
Accuracy	ppm		-1		1	Over the operational range
Stability	ppb			280		Over the operational range
Output Level	V		0.6	1		External, back panel
Output Impedance	Ohms			50		

External reference input						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Frequency	MHz			10		
Level	V		0.5		3	Peak-to-Peak
Impedance	Ohms			50		

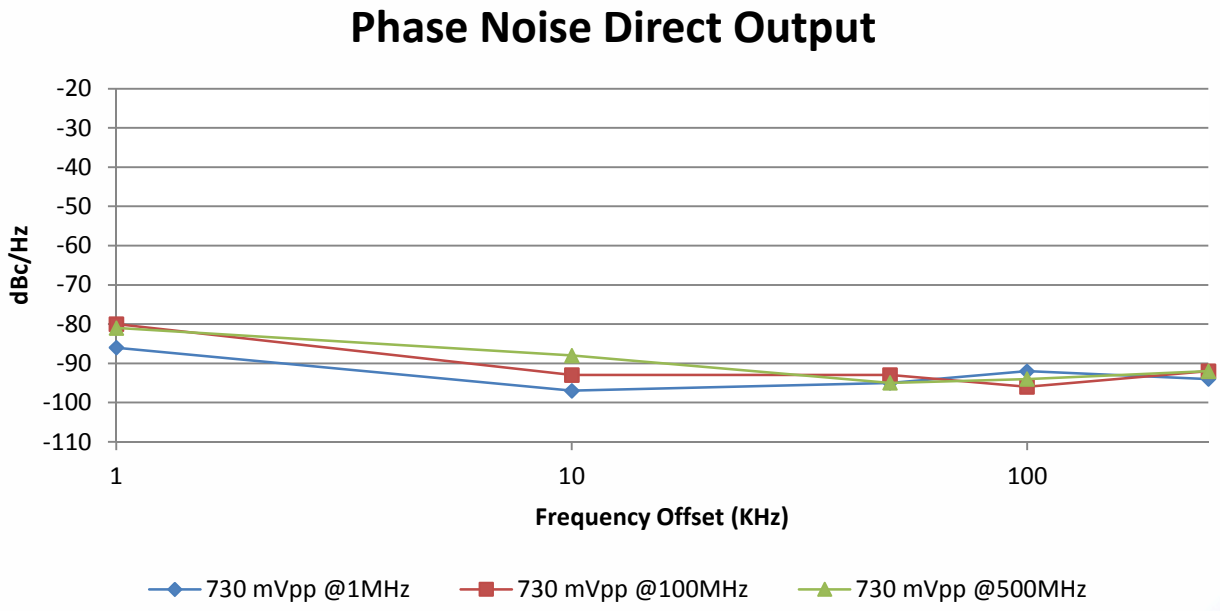
Sample clock						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Frequency	GHz		1.4		2.85	
Accuracy	%			1		
Output Level	mV				200	Rear panel, Peak-to-Peak
Output Impedance	Ohms			50		

Sample sequencer (future software update)						
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
Sample Granularity	Sample		1024		1G	
Sample Length			1024		1G	
Segments			1			
Loops			1			
Sample Memory	GSa				1	1 Sample = 14 bits + 2 Markers

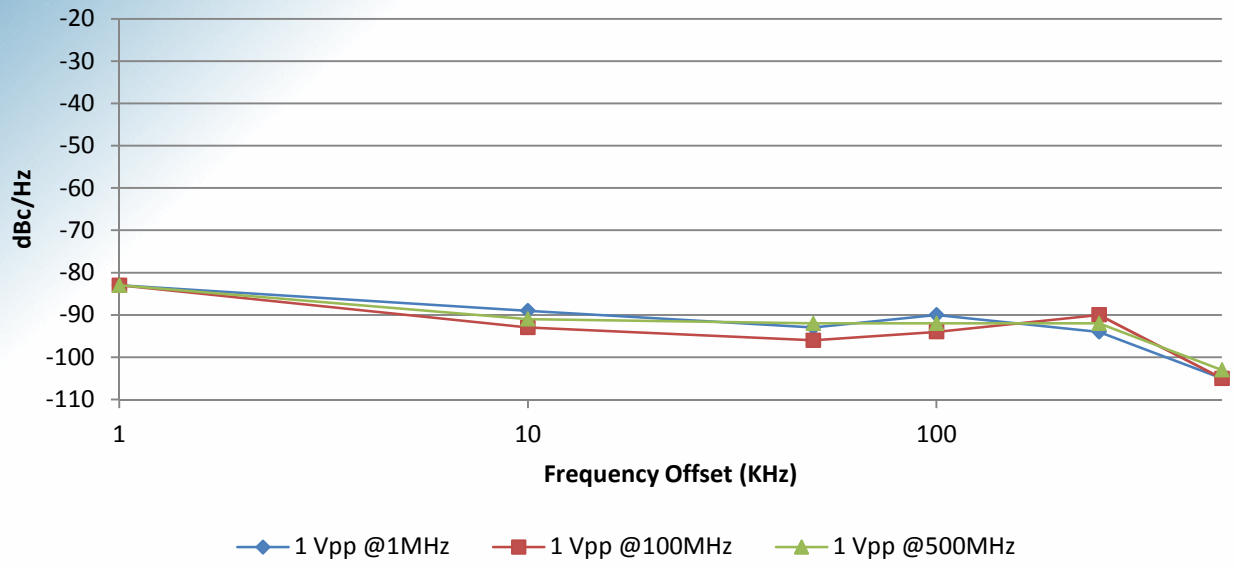
Parameter	**Unit**	**Symbol**	**Min.**	**Typ.**	**Max.**	**Comment**
General characteristics						
Power Supply Voltage	V		11.6	12	12.4	External power adapter
Power Supply Current	A		2	2.8	3	
Power Consumption	W			36		
Operating Temperature	°C		10		35	



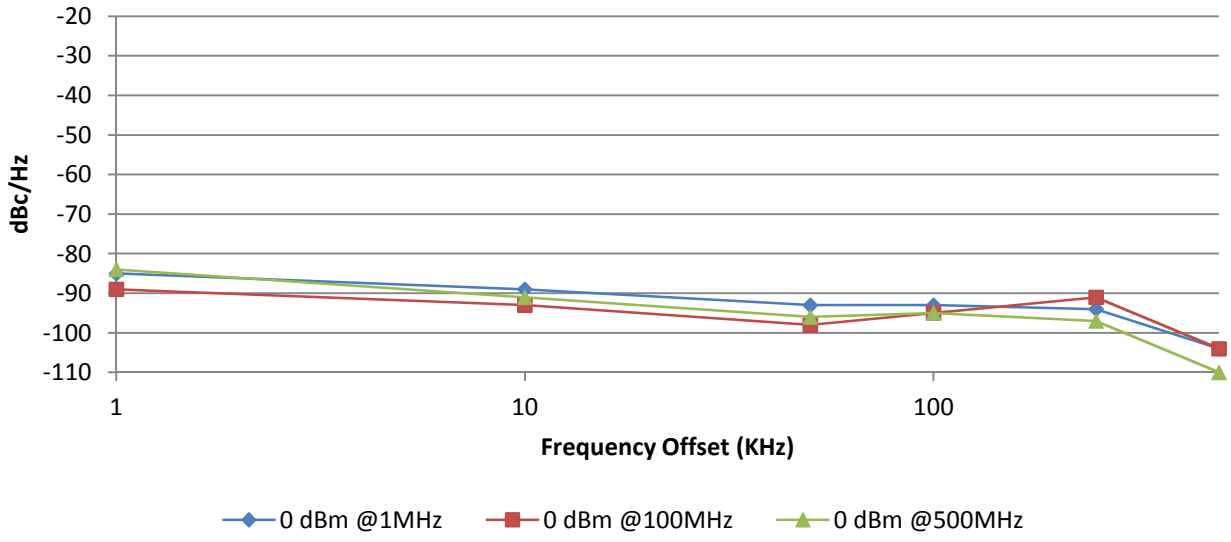
Measured on the DAC Clock SMA Output.



Phase Noise DC Output



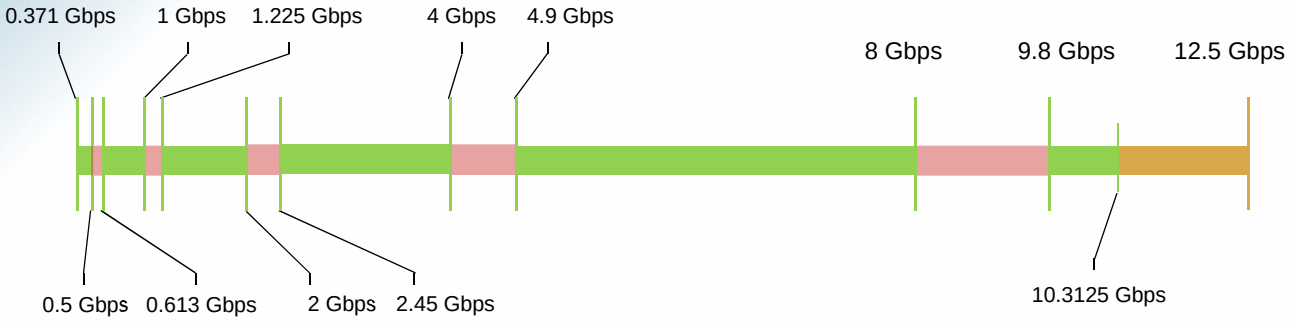
Phase Noise AC Output



BPG Outputs

Parameter	Unit	Symbol	Min.	Typ.	Max.	Comment
Impedance	Ω			50		
Output Level Minimum	mV		230		270	Single Ended, Peak-to-Peak, at 5 Gbps
Output Level Maximum	mV		700		730	Single Ended, Peak-to-Peak, at 5 Gbps
Output Level Steps				16		
Pre-Emphasis	dB		0		6.02	20 steps
Post-Emphasis	dB		0		12.96	31 steps
Jitter RMS	ps			5	6	At 5 Gbps, PRBS31, SQUARE2 for trigger.
Rise/Fall Time	ps			66	70	At 5 Gbps, PRBS31, SQUARE2 for trigger.
Crossing	%			50	52	At 5 Gbps, full output swing.
Duty Cycle	%			50		At 5 Gbps, full output swing.
Inter-Channel Skew	ps			20	30	20 ps max at 12.5 Gbps.
Output pattern	ITU-T (CCITT) conform PRBS patterns at a length of: 2^7-1, 2^9-1, 2^{10}-1, 2^{11}-1, 2^{13}-1, 2^{15}-1, 2^{20}-1, 2^{23}-1, 2^{31}-1 Additional SQUARE2 and SQUARE32 0-1 patterns: line rate divided by 2 and 32.					
Bit Rate (Range 1)	Gbps		0.372		0.5	
Bit Rate (Range 2)	Gbps		0.613		1	
Bit Rate (Range 3)	Gbps		1.225		2	
Bit Rate (Range 4)	Gbps		2.45		4	
Bit Rate (Range 5)	Gbps		4.9		8	
Bit Rate (Range 6)	Gbps		9.8		10.3125	Overclock up to 12.5 Gbps possible.
Bitrate resolution	Kbps			100		
Wordrame Trigger Division			32		2^{32}-1	Of internal clock cycles. 32 means 32 x (pattern length). Uses the AWG Trigger 2 as an output.
Wordrame Trigger Level	V		2.1	2.5		LVCMOS25
Wordframe Jitter	ps			150		Peak-to-Peak
PRBS Clock Input Level	dBm		-5		10	50 Ω, AC coupled
PRBS Clock Input Frequency	Mhz		60		2800	Using the internal divider

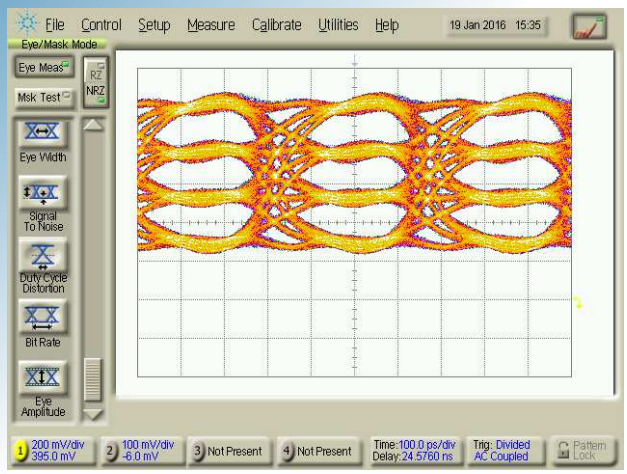
Bit Rate Ranges



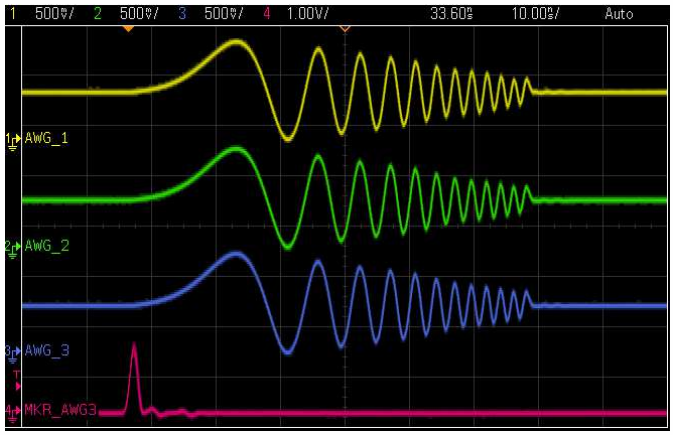
Pseudo Random Binary Sequence Pattern Types

Name	Polynomial	Length
$PRBS2^{7}$-1	$1 + X^{6} + X^{7}$	2^{7} - 1 bits
$PRBS2^{9}$-1	$1 + X^{9} + X^{5}$	2^{9} - 1 bits
$PRBS2^{10}$-1	$1 + X^{10} + X^{7}$	2^{10} - 1 bits
$PRBS2^{11}$-1	$1 + X^{11} + X^{9}$	2^{11} - 1 bits
$PRBS2^{13}$-1	$1 + X^{13} + X^{12} + X^{11} + X^{8}$	2^{13} - 1 bits
$PRBS2^{15}$-1	$1 + X^{14} + X^{15}$	2^{15} - 1 bits
$PRBS2^{20}$-1	$1 + X^{17} + X^{20}$	2^{20} - 1 bits
$PRBS2^{23}$-1	$1 + X^{18} + X^{23}$	2^{23} - 1 bits
$PRBS2^{31}$-1	$1 + X^{28} + X^{31}$	2^{31} - 1 bits

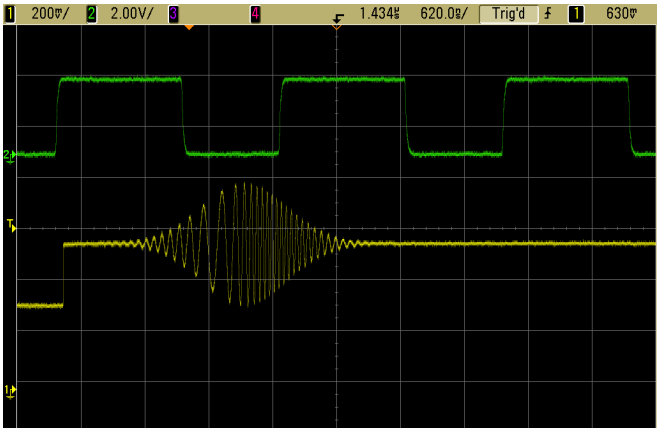
Typical Output Waveforms (AWG)



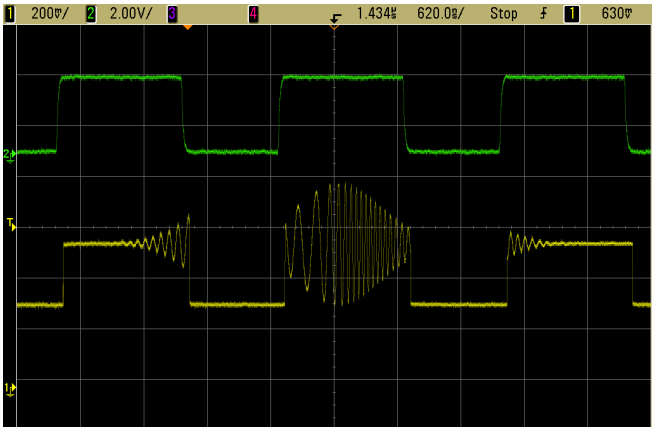
2.8 Gbps PAM-4 signal, DC Output



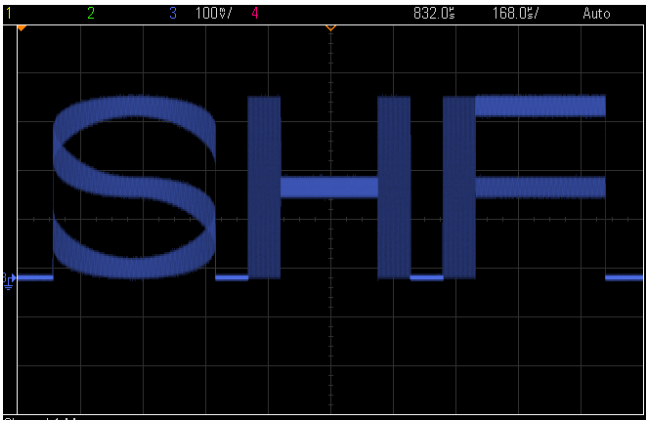
Frequency and phase synchronization of three SHF 19120 A



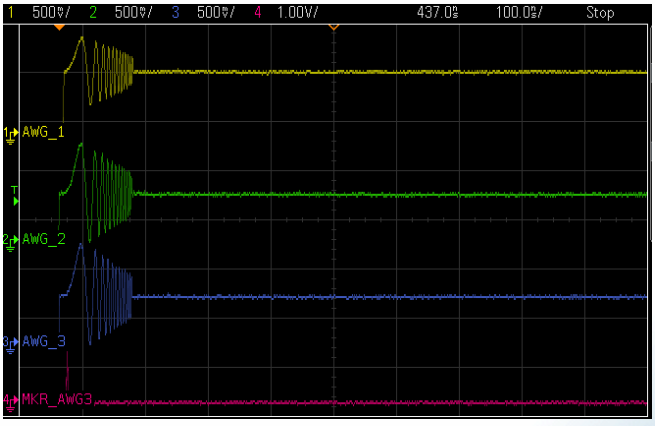
Edge-triggered signal generation.



Level-gated trigger signal generation.

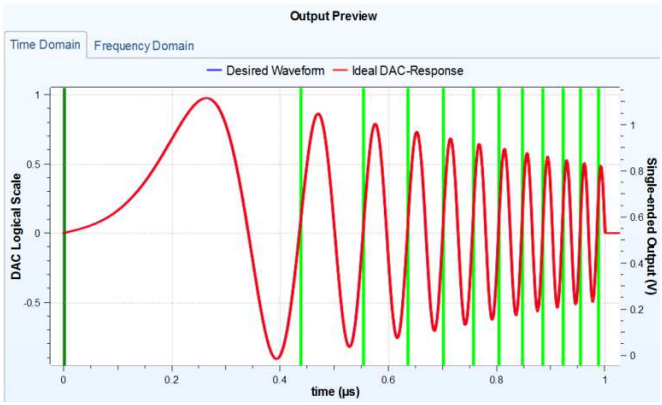


“SHF” writing

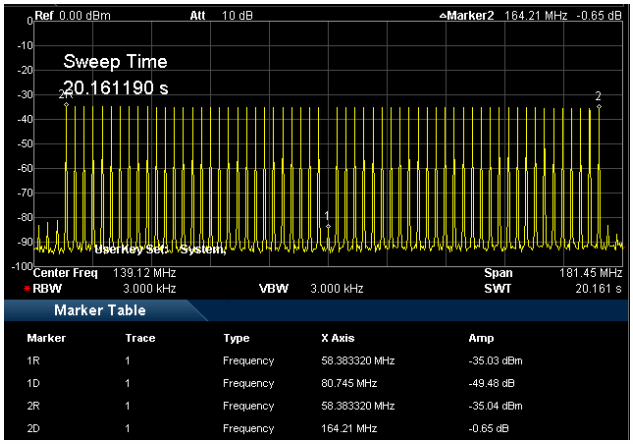


Burst mode of three synchronized SHF 19120 A

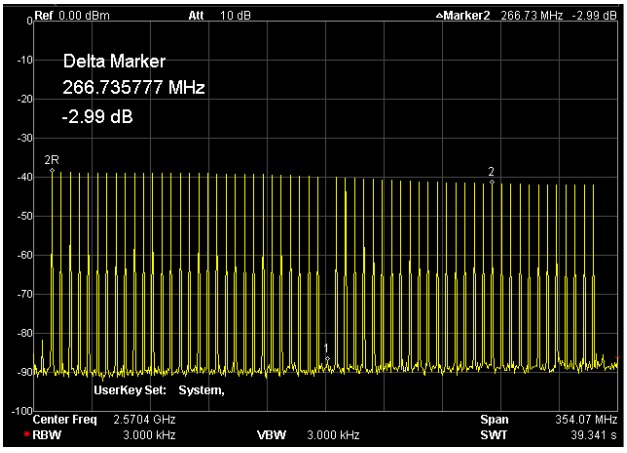
Signal with markers: marker output 1 for each rising part of signal, marker output 2 for the signal start.



Screenshot from the SHF Control Center preview of the signal shown on the left.

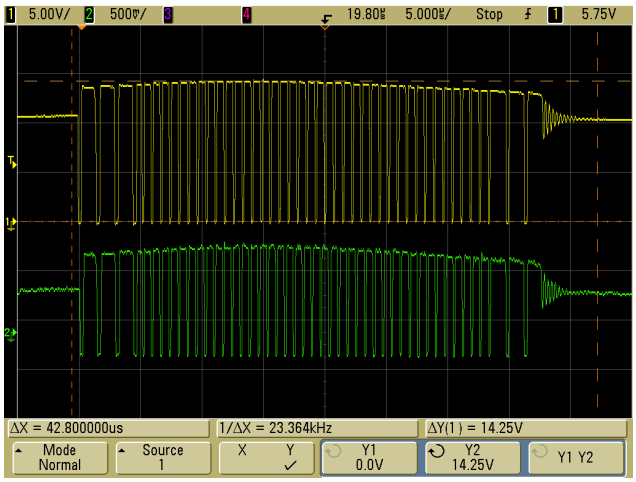


Multiple-Carrier Signal Noise-Power Ratio, AC Output



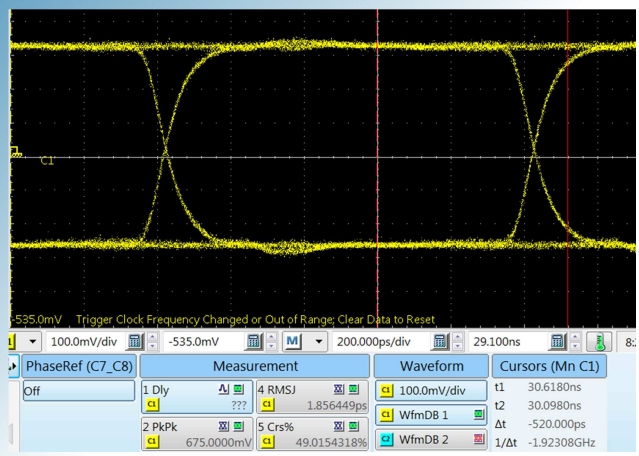
Multiple-Carrier Signal Noise-Power Ratio in Double Interpolation Mode, AC Output.

Delta marker shows the sin(x)/x bandwidth drop



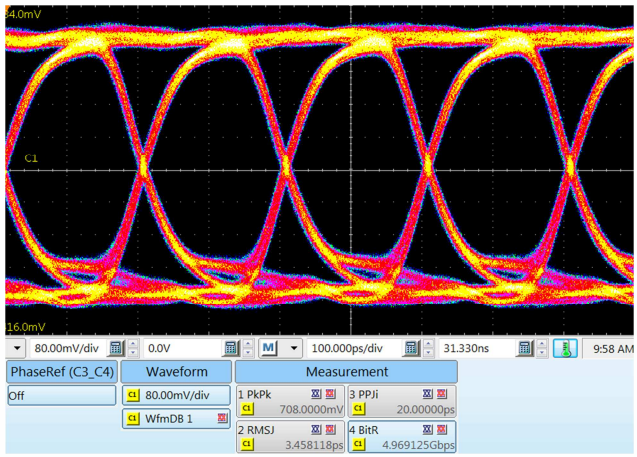
Original (yellow) and AWG waveform (green) after import. Inductor voltage of a Ćuk converter.

Typical Output Waveforms (BPG)



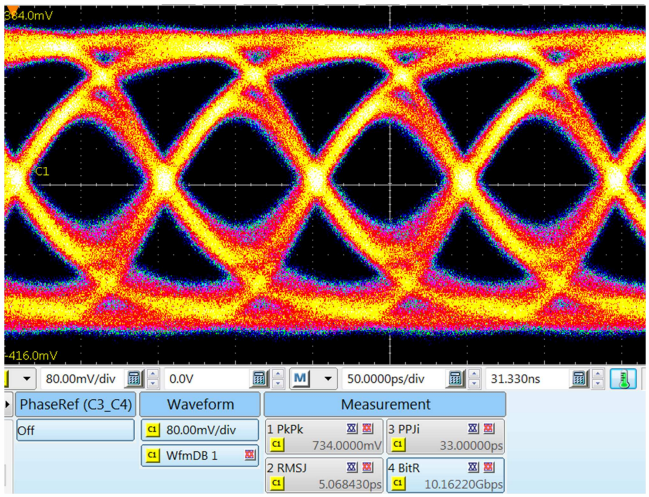
1 Gbps PRBS^{31}-1

POST cursor = 0dB PRE cursor = 0dB, Amplitude = 715 mVpp



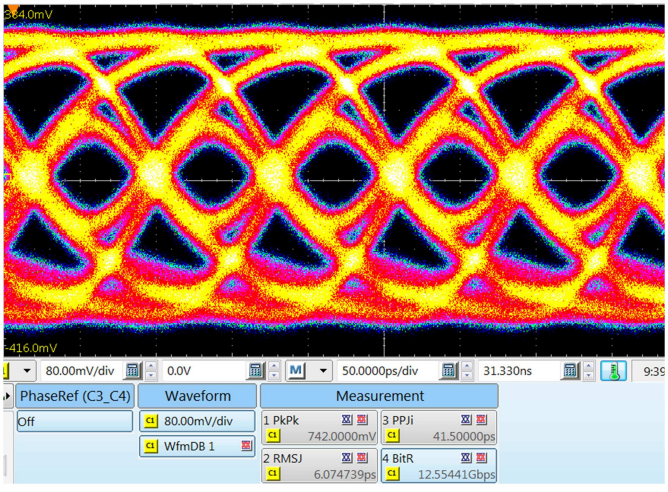
5 Gbps PRBS^{31}-1

POST cursor = 0dB PRE cursor = 0dB, Amplitude = 715 mVpp



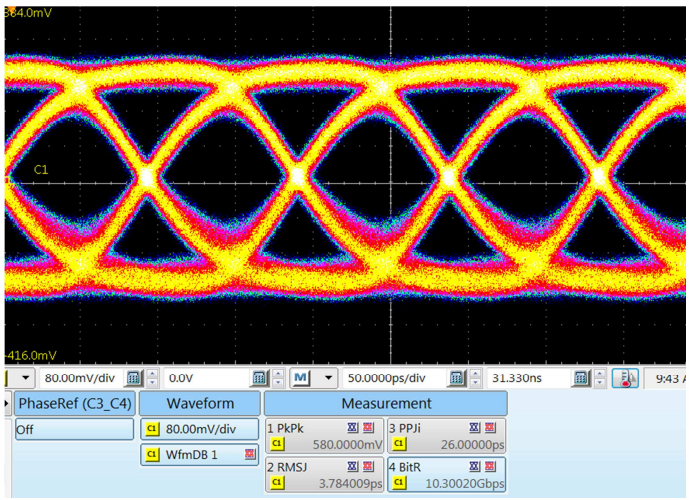
10.3125 Gbps PRBS^{31}-1

POST cursor = 0dB PRE cursor = 0dB, Amplitude = 715 mVpp



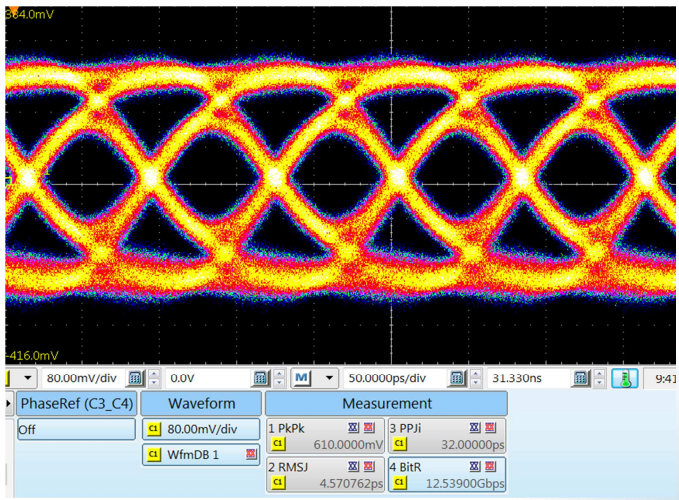
12.5 Gbps PRBS^{31}-1

POST cursor = 0dB PRE cursor = 0dB, Amplitude = 715 mVpp



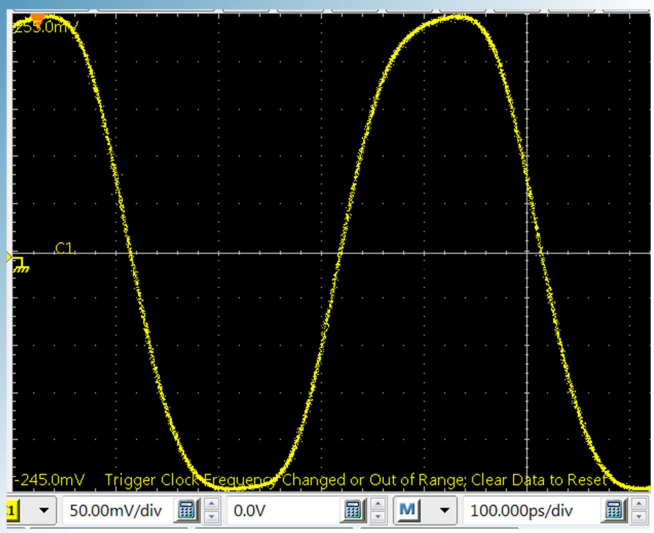
10.3125 Gbps PRBS^{31}-1

POST cursor = 1.6dB PRE cursor = 1.6dB, Amplitude = 635 mVpp

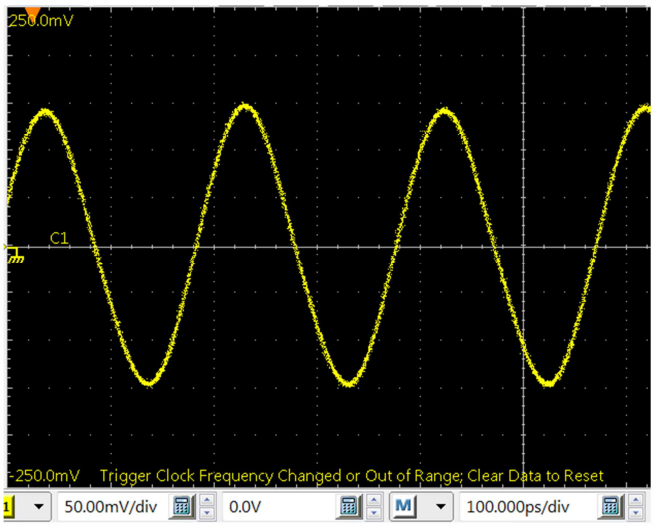


12.5 Gbps PRBS^{31}-1

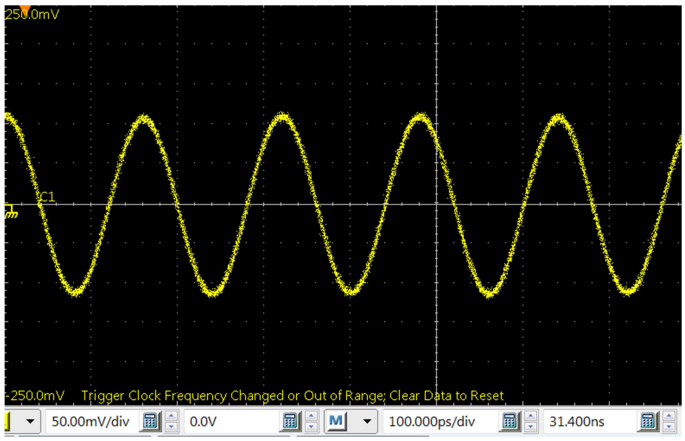
POST cursor = 1.6dB PRE cursor = 1.6dB, Amplitude = 635 mVpp



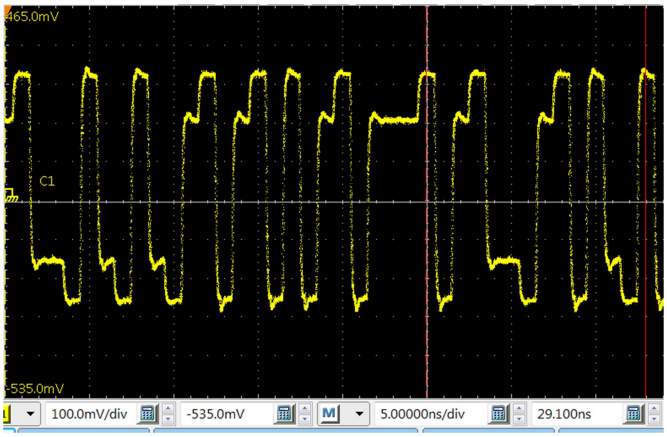
SQUARE 2 pattern on the 5 Gbps line rate



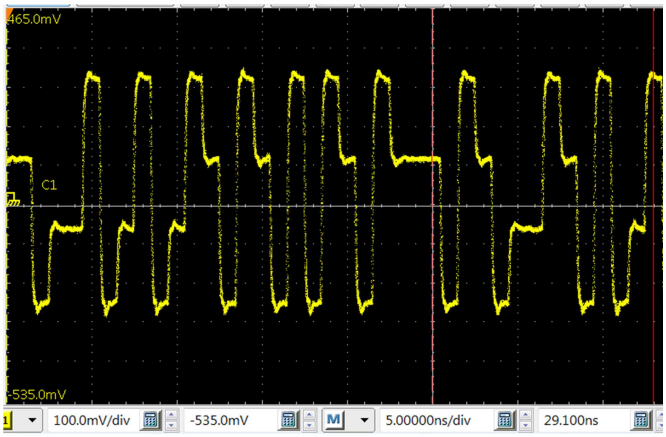
SQUARE 2 pattern on the 10.3125 Gbps line rate



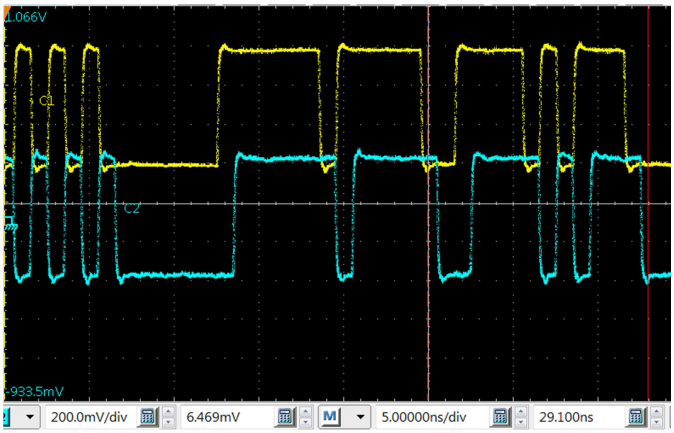
SQUARE 2 pattern on the 12.5 Gbps line rate



PRE Emphasis – Max. value (1 Gbps, PRBS^7-1)



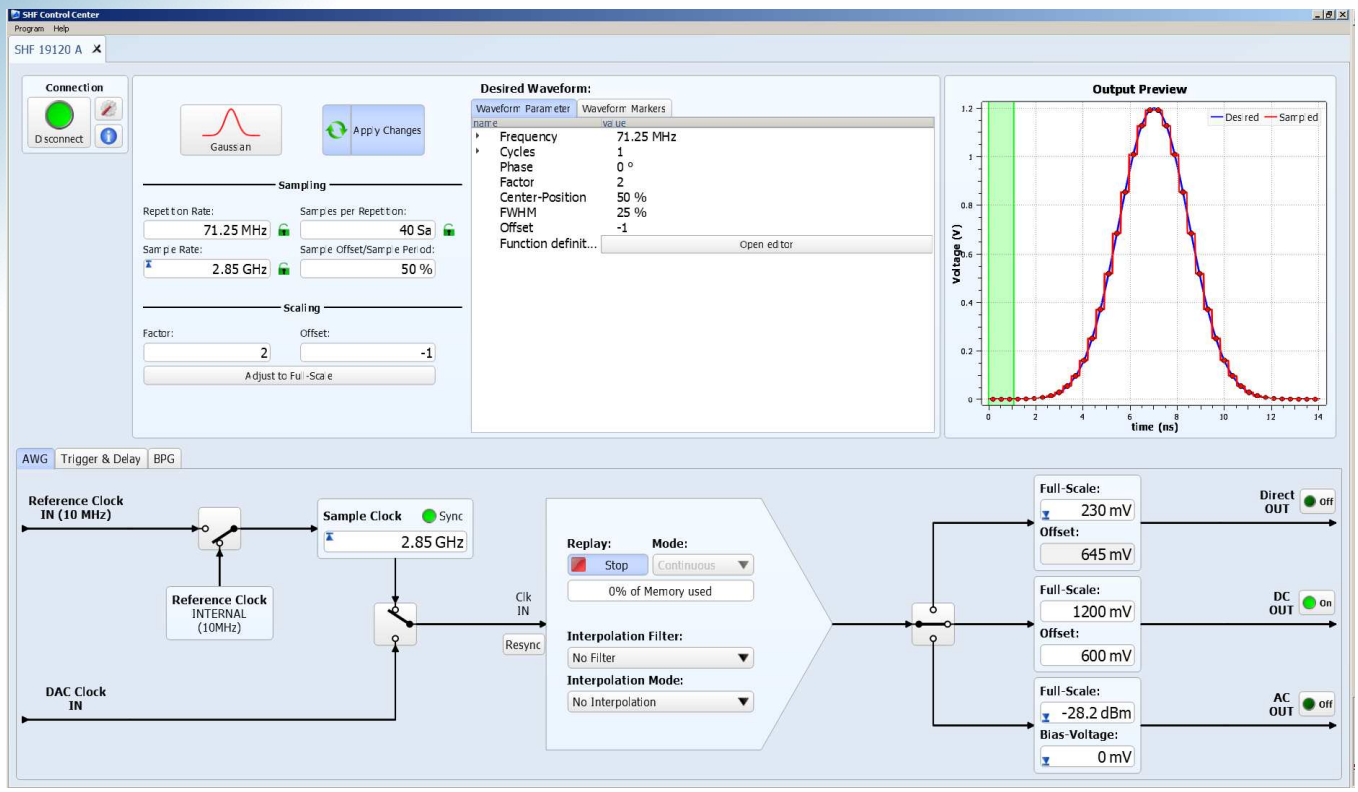
POST Emphasis – Max. value (1 Gbps, PRBS^7-1)



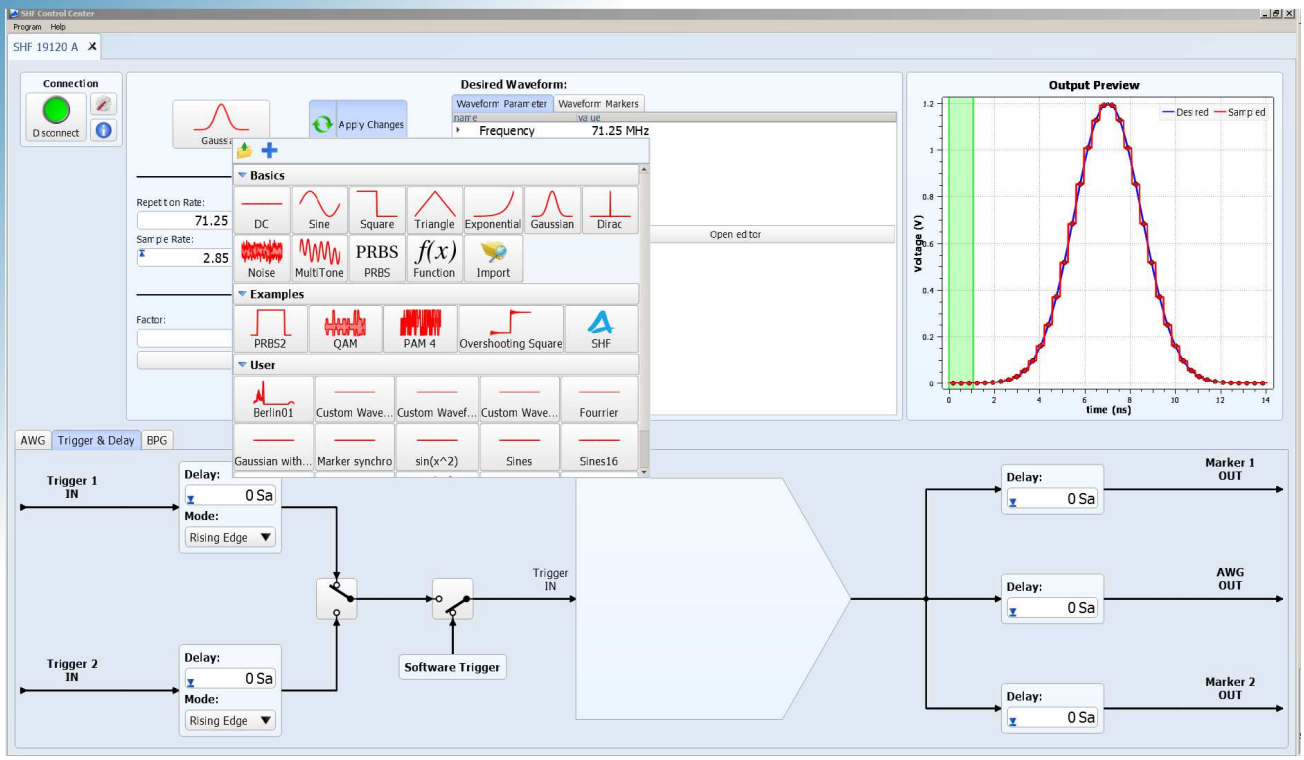
1 Bit Pattern Shift (1 Gbps, PRBS^7-1 ; ch1 and ch2)

Software

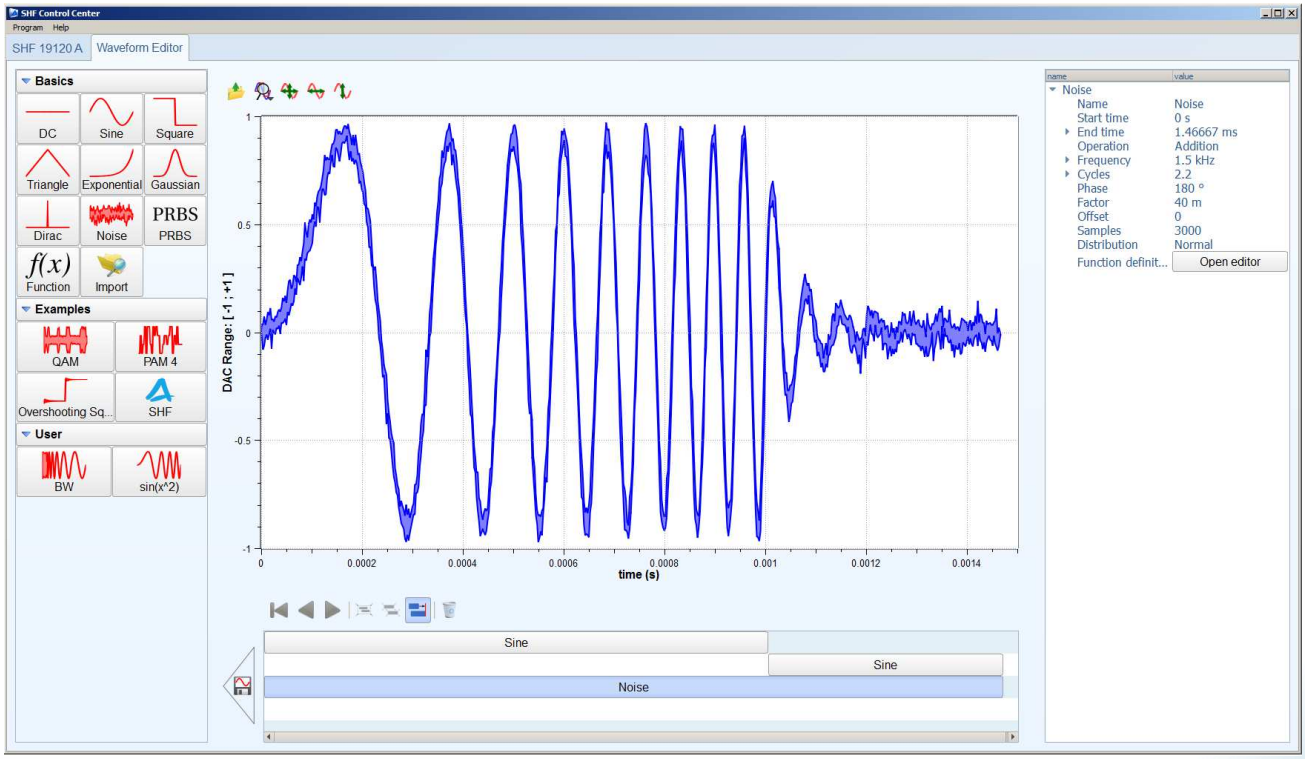
The SHF 19120 A is operated via an Ethernet connection with the SHF Control Center software. An embedded version of the software comes pre-installed on the instrument. It can be used without a PC, simply by connecting an HDMI monitor, a keyboard and a mouse (USB) to the rear panel.



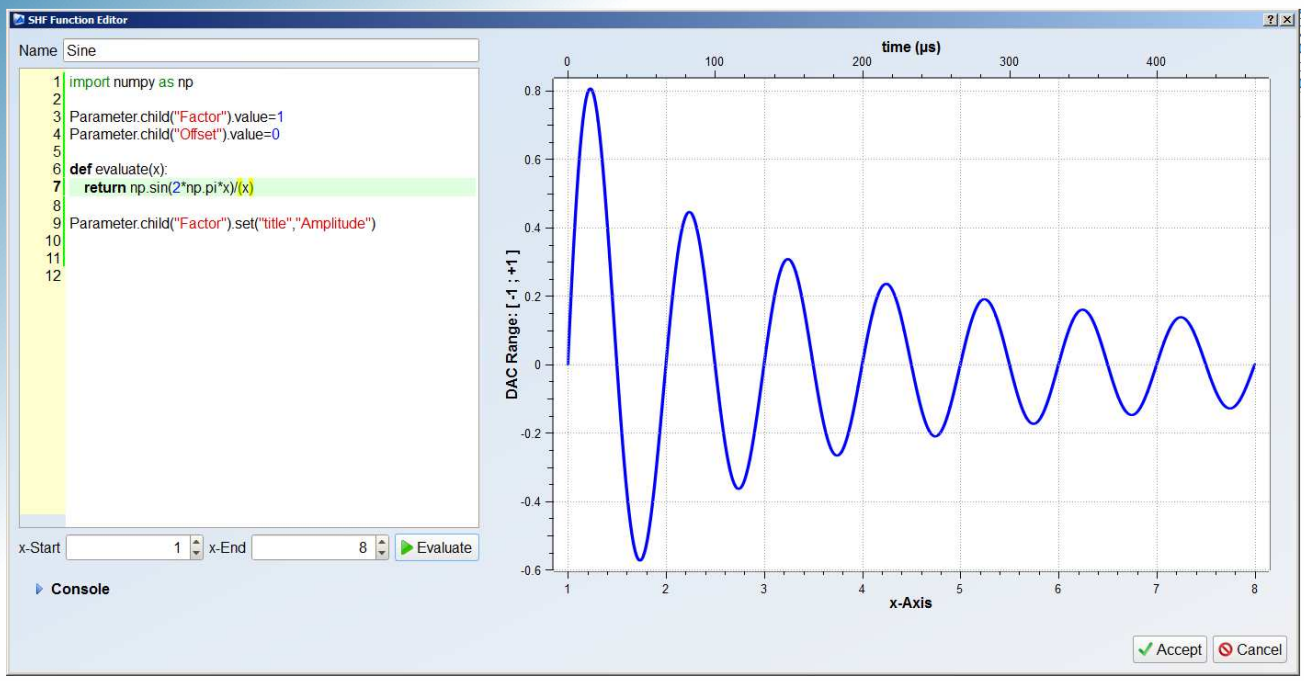
SHF Control Center Software



SHF Control Center Software: Trigger Settings and Waveform Library pop-up



SHF Control Center Software: Waveform Editor.

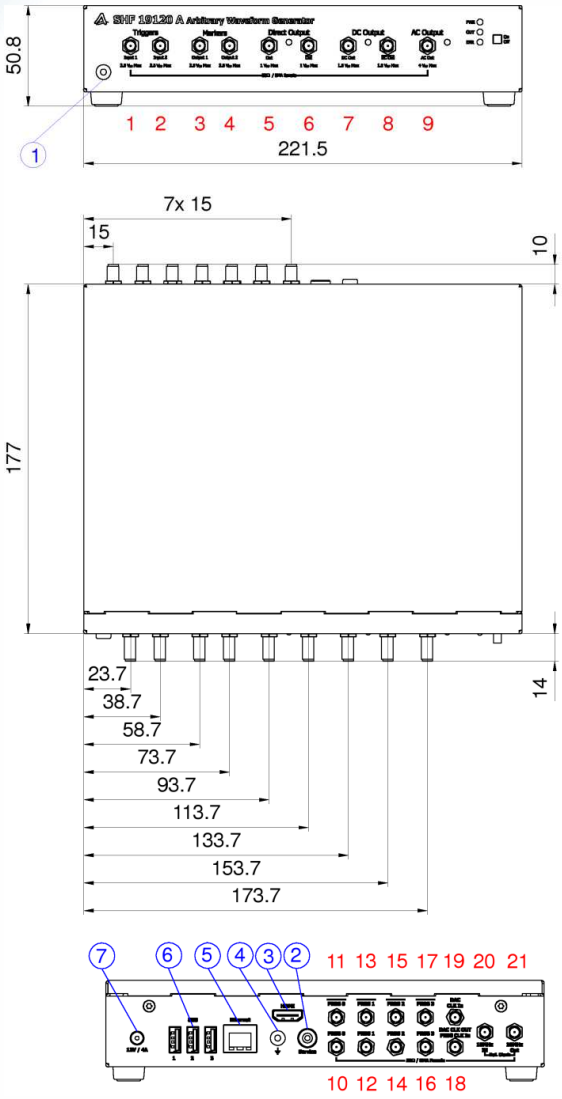


SHF Control Center Software: Equation Editor

	Channel 0	Channel 1	Channel 2	Channel 3
Bitrate	6.000 Gbps	6.000 Gbps	6.000 Gbps	6.000 Gbps
Type	PRBS 2^7-1	PRBS 2^{23}-1	PRBS 2^{31}-1	SQUARE2
Polarity	Non-Inverted	Non-Inverted	Non-Inverted	Non-Inverted
Delay	0 Bits	16 Bits	0 Bits	0 Bits
Amplitude	720 mV	720 mV	720 mV	720 mV
Pre-emphasis: Precursor	0 dB	0 dB	0 dB	0 dB
Pre-emphasis: Postcursor	0 dB	0 dB	0 dB	0 dB
Output	On	On	On	On

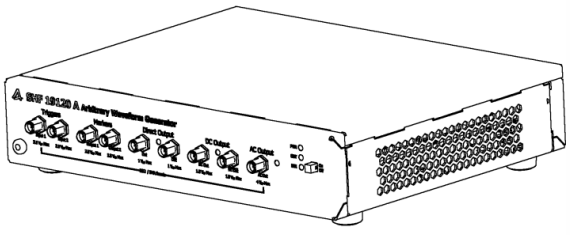
SHF Control Center Software: Detail of the BPG Controls

Outline Drawing



Pos	Designation	Connector
1	Trigger Input 1	SMA
2	Trigger Input 2	SMA
3	Marker Output 1	SMA
4	Marker Output 2	SMA
5	Direct Output Out	SMA
6	Direct Output $\overline{\text{Out}}$	SMA
7	DC Output DC Out	SMA
8	DC Output $\overline{\text{DC Out}}$	SMA
9	AC Output AC Out	SMA
10	PRBS 0	SMA
11	$\overline{\text{PRBS 0}}$	SMA
12	PRBS 1	SMA
13	$\overline{\text{PRBS 1}}$	SMA
14	PRBS 2	SMA
15	$\overline{\text{PRBS 2}}$	SMA
16	PRBS 3	SMA
17	$\overline{\text{PRBS 3}}$	SMA
18	DAC CLK OUT / PRBS CLK IN	SMA
19	DAC CLK IN	SMA
20	10MHz In	SMA
21	10MHz Out	SMA

Pos	Designation
1	GND
2	Service
3	HDMI
4	GND
5	Ethernet
6	USB
7	Power In



All dimensions are specified in millimeters (mm).