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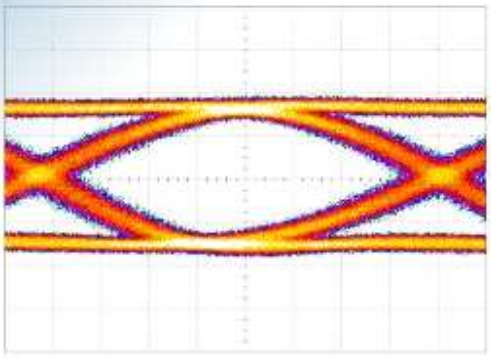
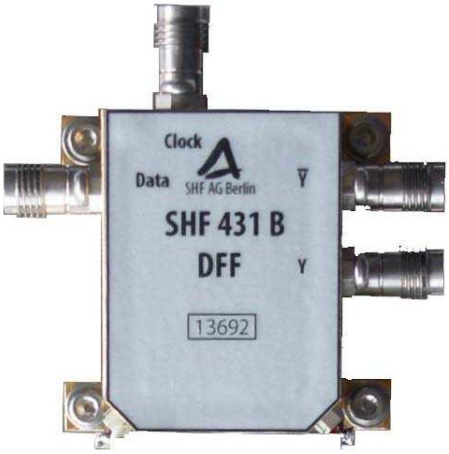


Datasheet

SHF 431B

55 Gbps

D-type Flip Flop (DFF)



Description

The SHF 431B is a D-type flip-flop (DFF) module capable of broadband operation up to 55 Gbps. AC-coupled and 50 Ω terminated data and clock inputs ensure proper line termination and uncomplicated application. Optimum bias point for the data input can be set using the data bias connector.

Features

- Broadband operation up to 55 Gbps
- Differential output, 250 mV_{pp} single ended output swing
- Low power consumption
- single ended operation (data and clock input)

Applications

- OC-768/STM-256 applications
- Broadband test and measurement equipment

Option

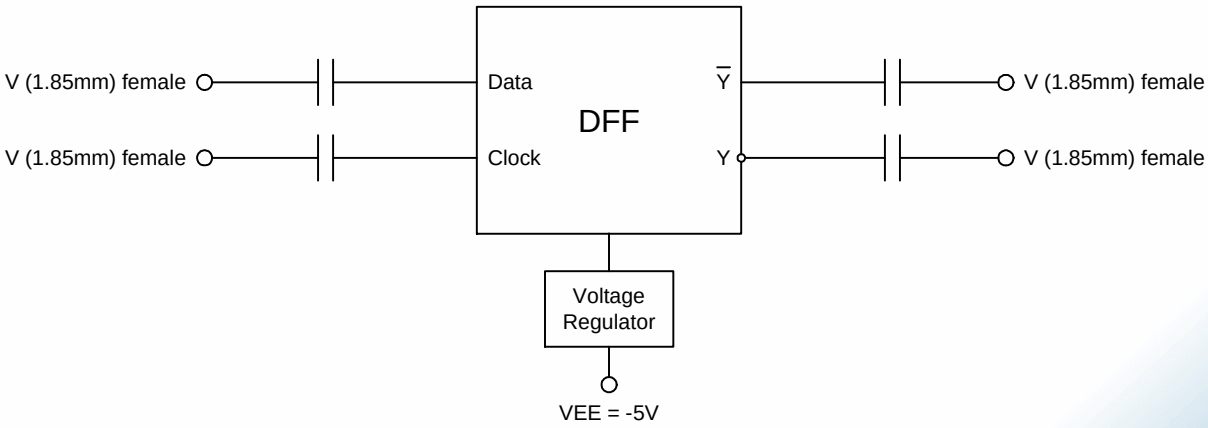
- Option bias adjust (BA): Module comes along with a wall power supply. One potentiometers to allow data bias to be adjusted without the need for additional power supplies.

Specifications

Parameter	Symbol	Unit	Min	Typ	Max	Conditions
Performance						
Minimum input data rate[1]	$R_{in,min}$	Gbps		5		500mV$_{pp}$ clock signal
Maximum input data rate	$R_{in,max}$	Gbps	50	55		500mV$_{pp}$ clock signal
Data input voltage	D_{in}	mV$_{pp}$	300		1000	Eye Height
Clock input frequency		GHz	5		50	
Clock input voltage	CLK_{in}	mV$_{pp}$	500		1000	
Input return loss	S_{11}	dB	5			
Single ended output swing		mV	250			Eye Amplitude, into 50 Ω load
Rise/Fall time	t_r/t_f	ps		9		20%/80%
RMS jitter		fs		400	600	
Output return loss	S_{22}	dB	5			
Data/Clock bias adjust		V	-5	-2.5	0	
Operating conditions						
Power supply	V_{EE}	V	-4.5	-5	-5.5	
Supply current	I_{EE}	mA		100		
Power consumption	T_d	mW		500		@ V_{EE} = -5V
Operating temperature	T_{op}	℃	10		50	
Dimensions		mm				59x40x18

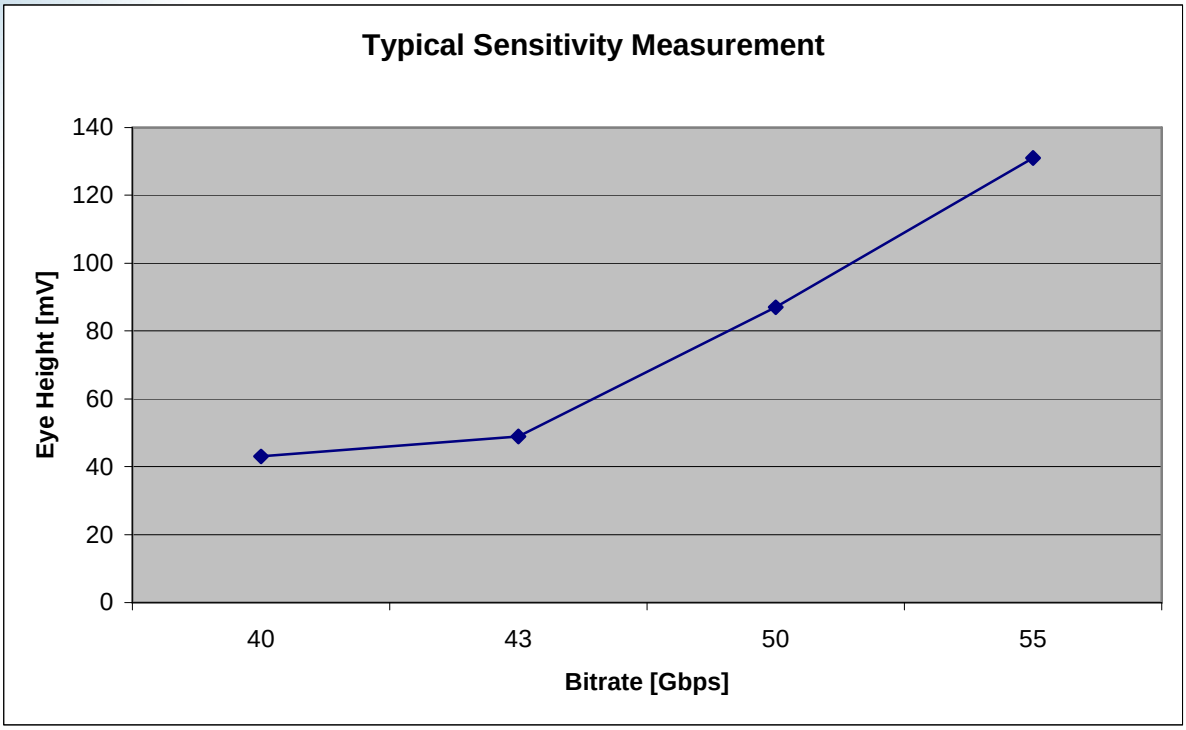
1) The theoretical limit is DC, practical limit depends on slew rate of clock signal.

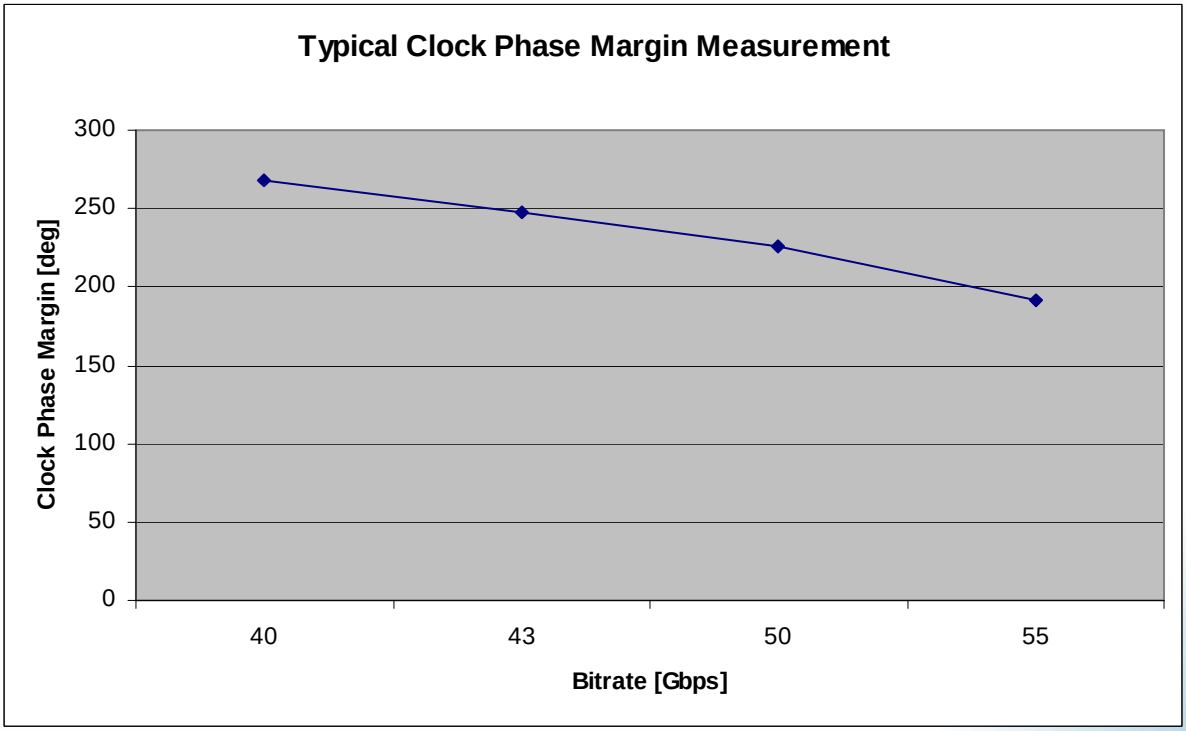
Block Diagram



Sensitivity and Clock Phase Margin Measurements

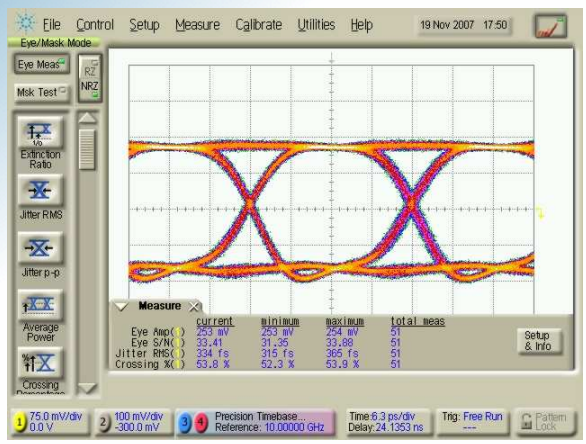
The measurements below have been performed using a SHF 12100A BPG (PRBS 2^{31}-1, $V_{amplitude}$ = 400 mV), a SHF 11100A Error Analyzer and an Agilent 86100B DCA with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A) to determine the eye height and jitter contribution of the input signal. In case of the sensitivity measurement the input signal has been reduced until a BER limit of 10-9 was achieved. For the CPM measurement the phase of the clock signal was varied until the BER reached the 10-9 limit.



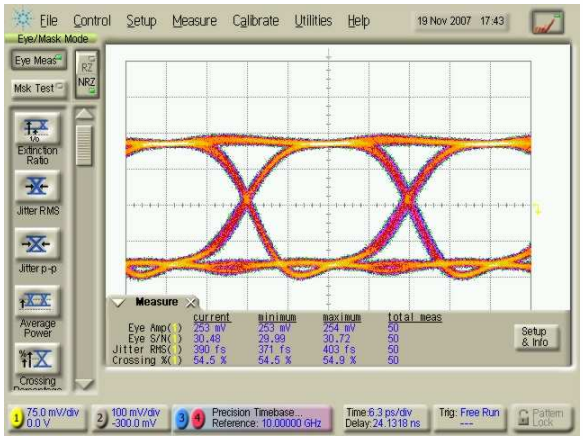


Output waveforms

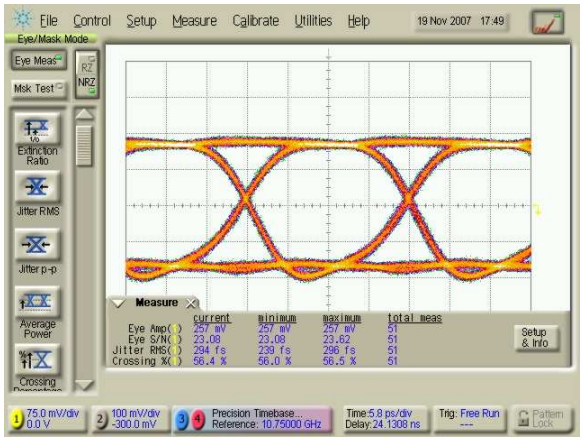
The measurements below have been performed using a SHF 12100A BPG (PRBS 2^{31}-1, $V_{amplitude}$ = 400 mV) and an Agilent 86100B DCA with Precision Time Base Module (86107A) and 70 GHz Sampling Head (86118A). The output of the DFF module has been connected to the DCA input with a 0.5 m microwave cable assembly.



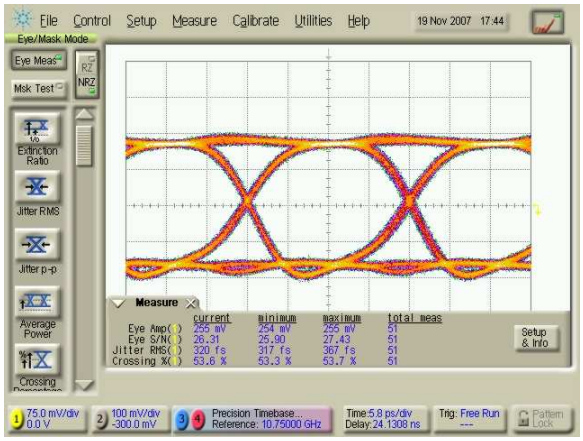
Y @ 40 Gbps



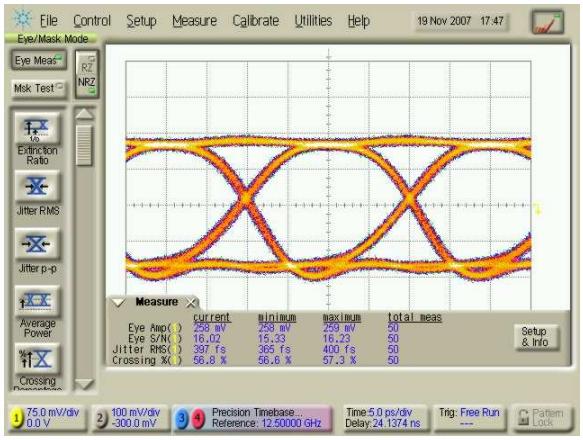
Y! @ 40 Gbps



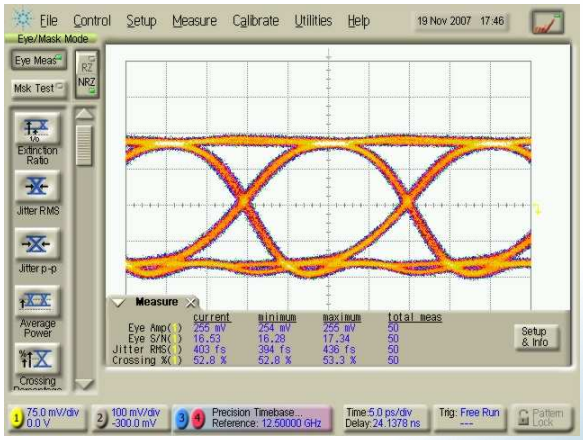
Y @ 43 Gbps



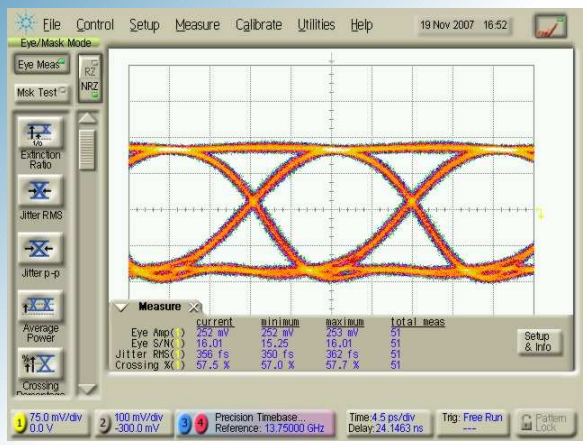
Y! @ 43 Gbps



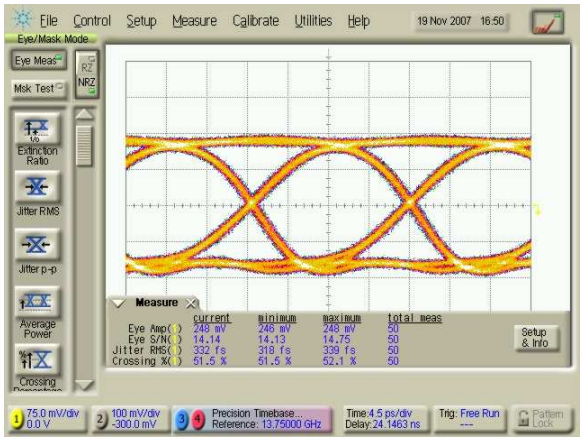
Y @ 50 Gbps



Y! @ 50 Gbps

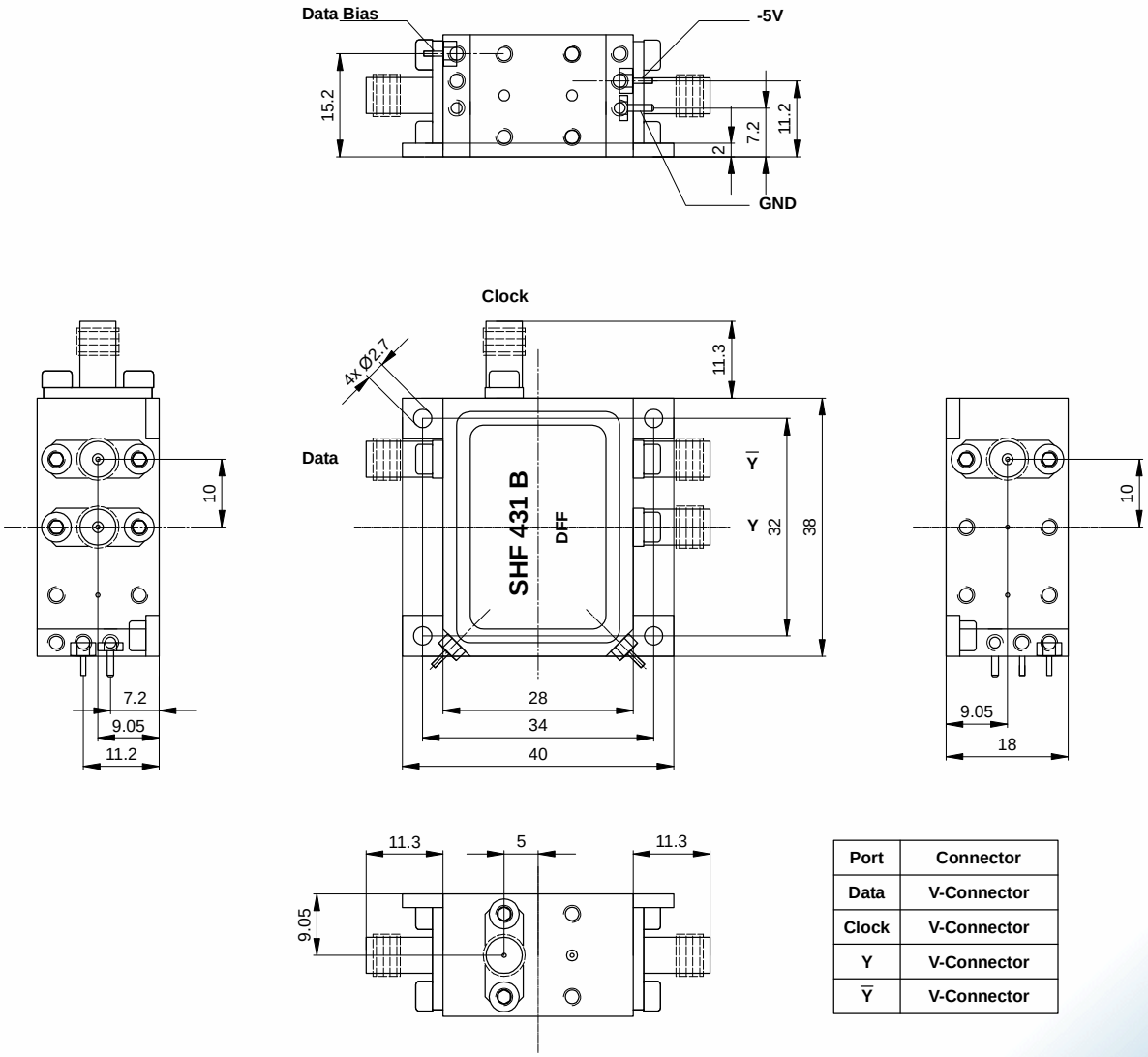


Y @ 55 Gbps



Y! @ 55 Gbps

Outline Drawing



Port	Connector
Data	V-Connector
Clock	V-Connector
Y	V-Connector
$\overline{Y}$	V-Connector